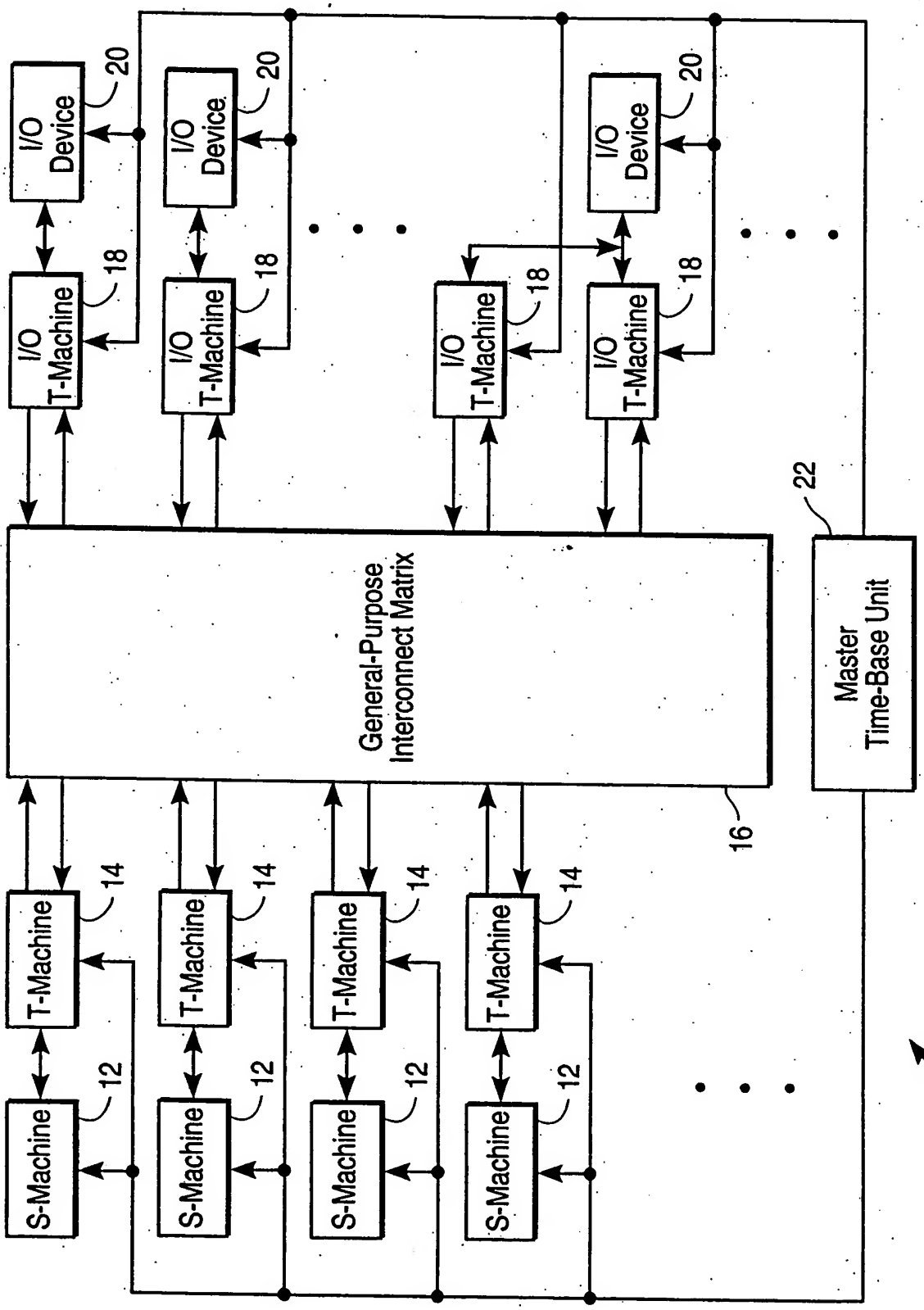
I/O Device
20
I/O T-Machine
18
General-Purpose Interconnect Matrix
16
Master Time-Base Unit
22
T-Machine
14
S-Machine
12
10

FIG. 1

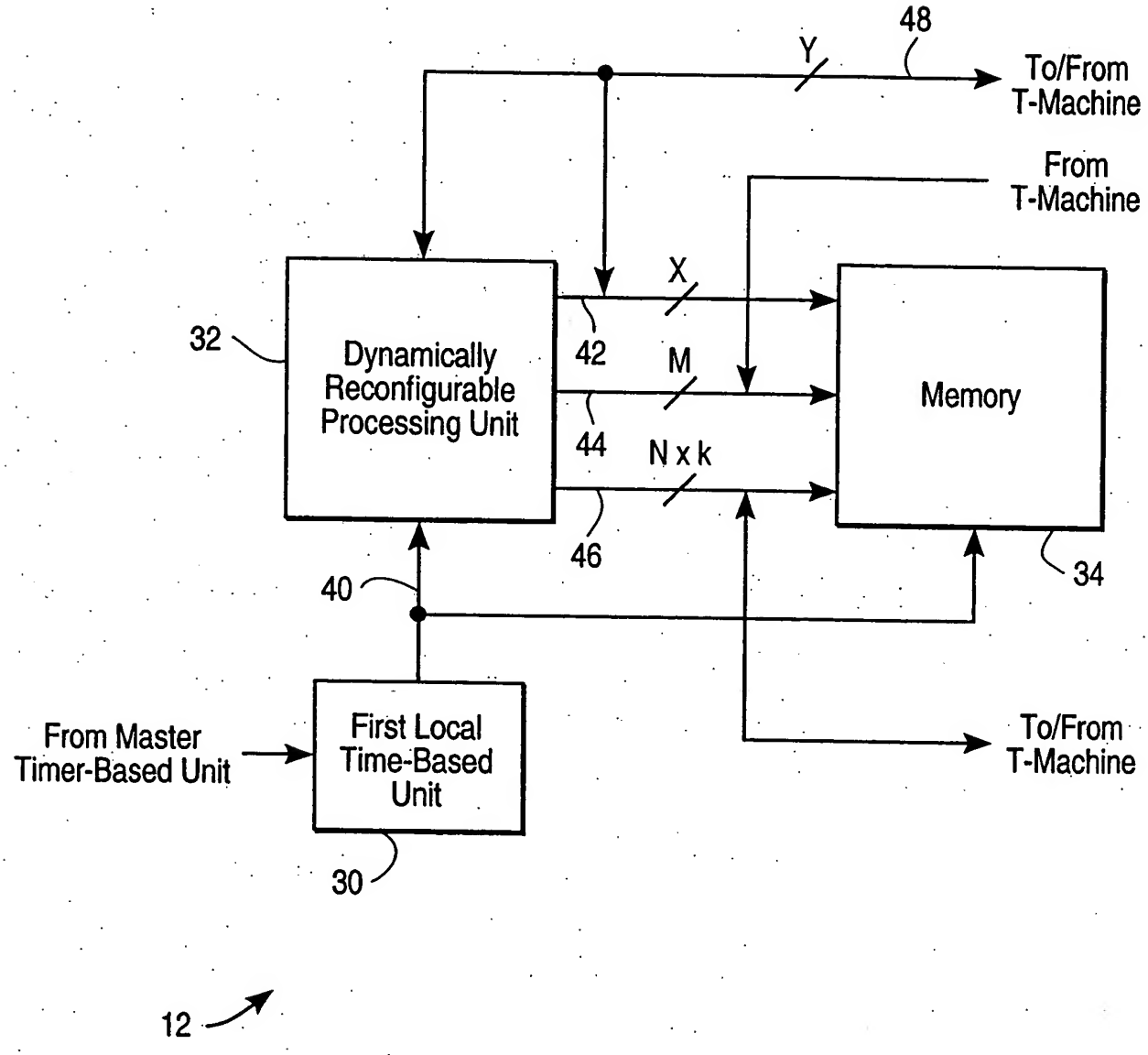
48
Y
To/From
T-Machine
From
T-Machine
X
32
Dynamically
Reconfigurable
Processing Unit
42
M
Memory
44
N x k
46
34
40
From Master
Timer-Based Unit
First Local
Time-Based
Unit
To/From
T-Machine
30
12

FIG. 2

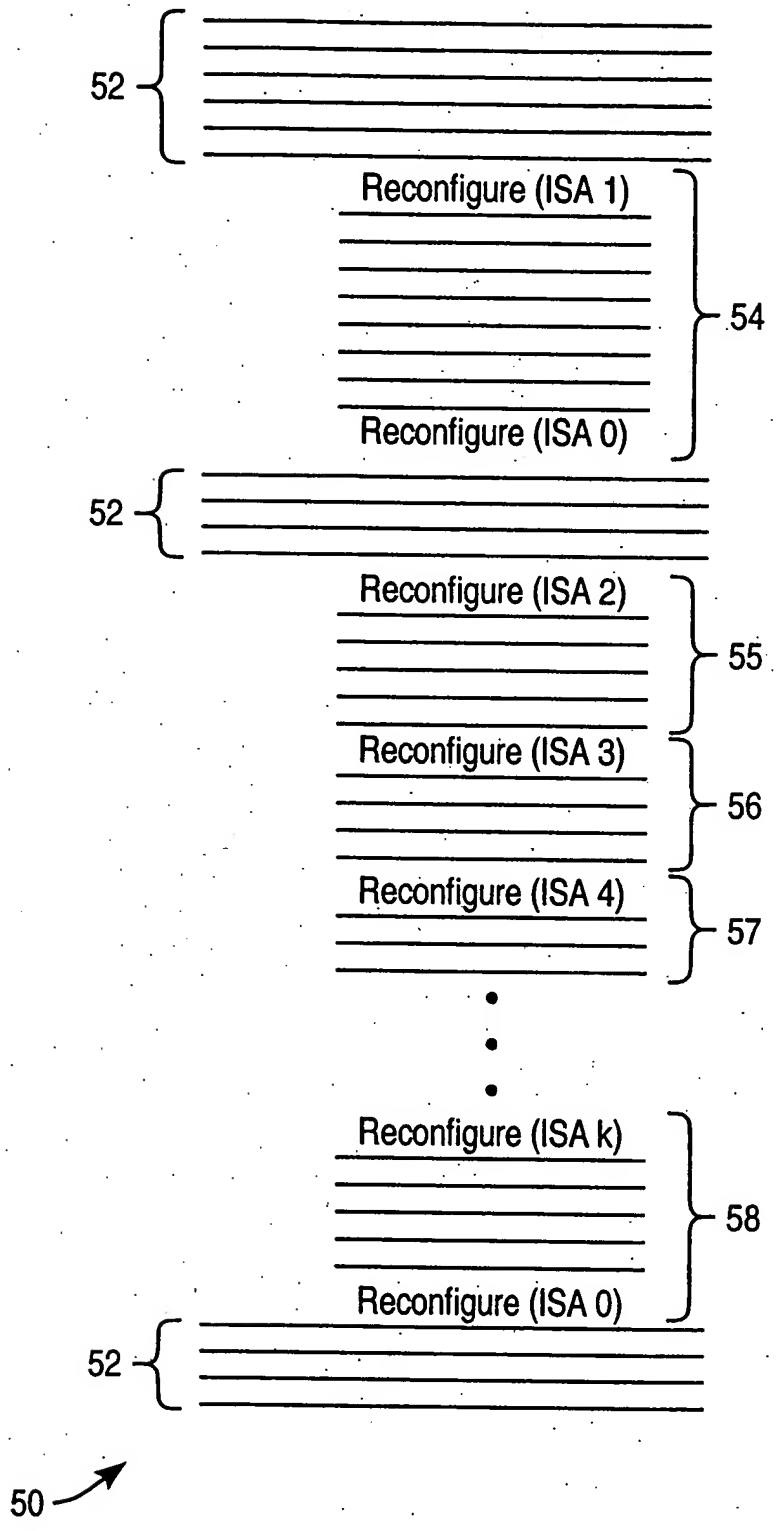
52
Reconfigure (ISA 1)
54
Reconfigure (ISA 0)
52
Reconfigure (ISA 2)
55
Reconfigure (ISA 3)
56
Reconfigure (ISA 4)
57
Reconfigure (ISA k)
58
Reconfigure (ISA 0)
52
50

FIG. 3A

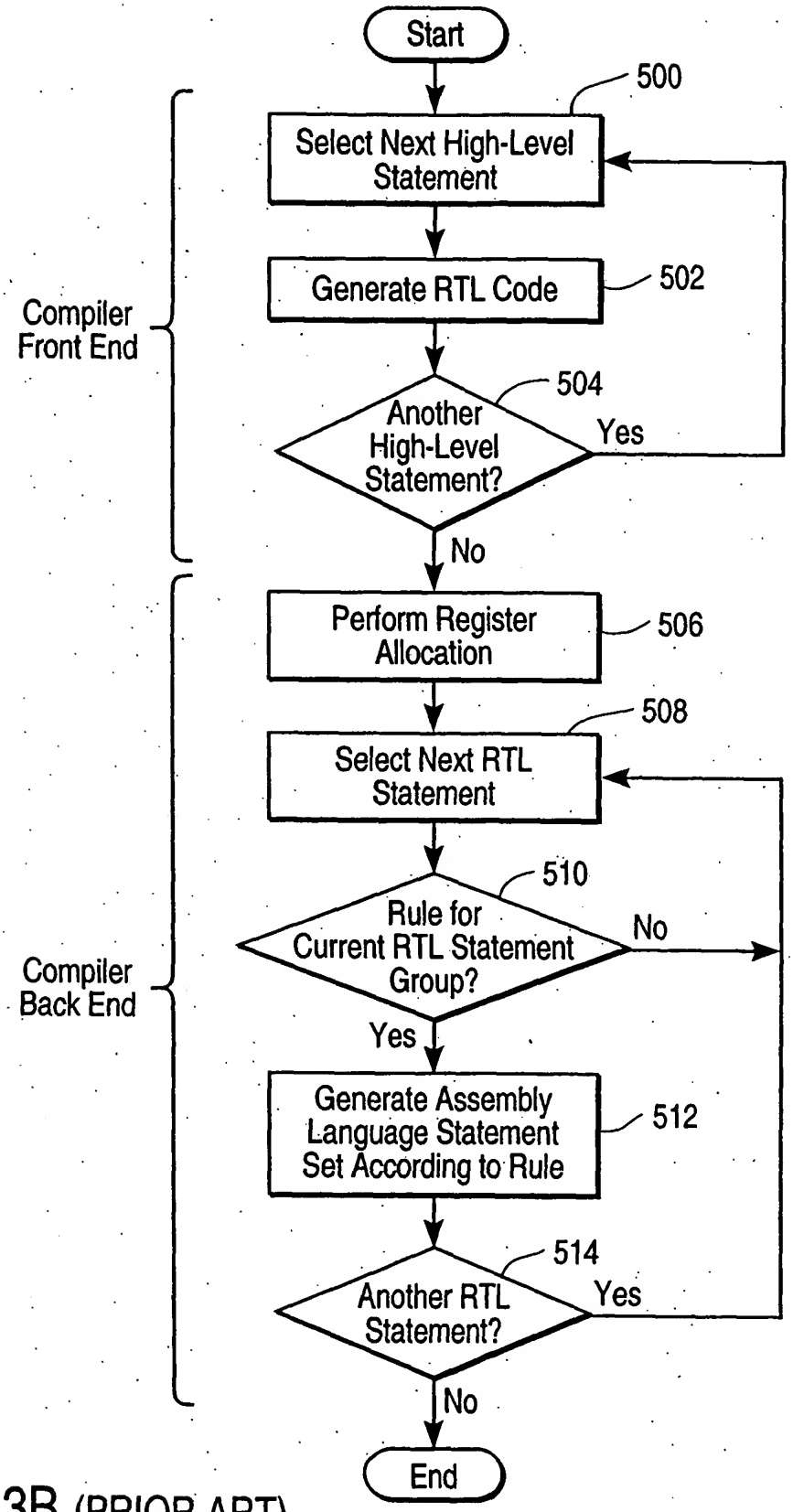

FIG. 3B (PRIOR ART)

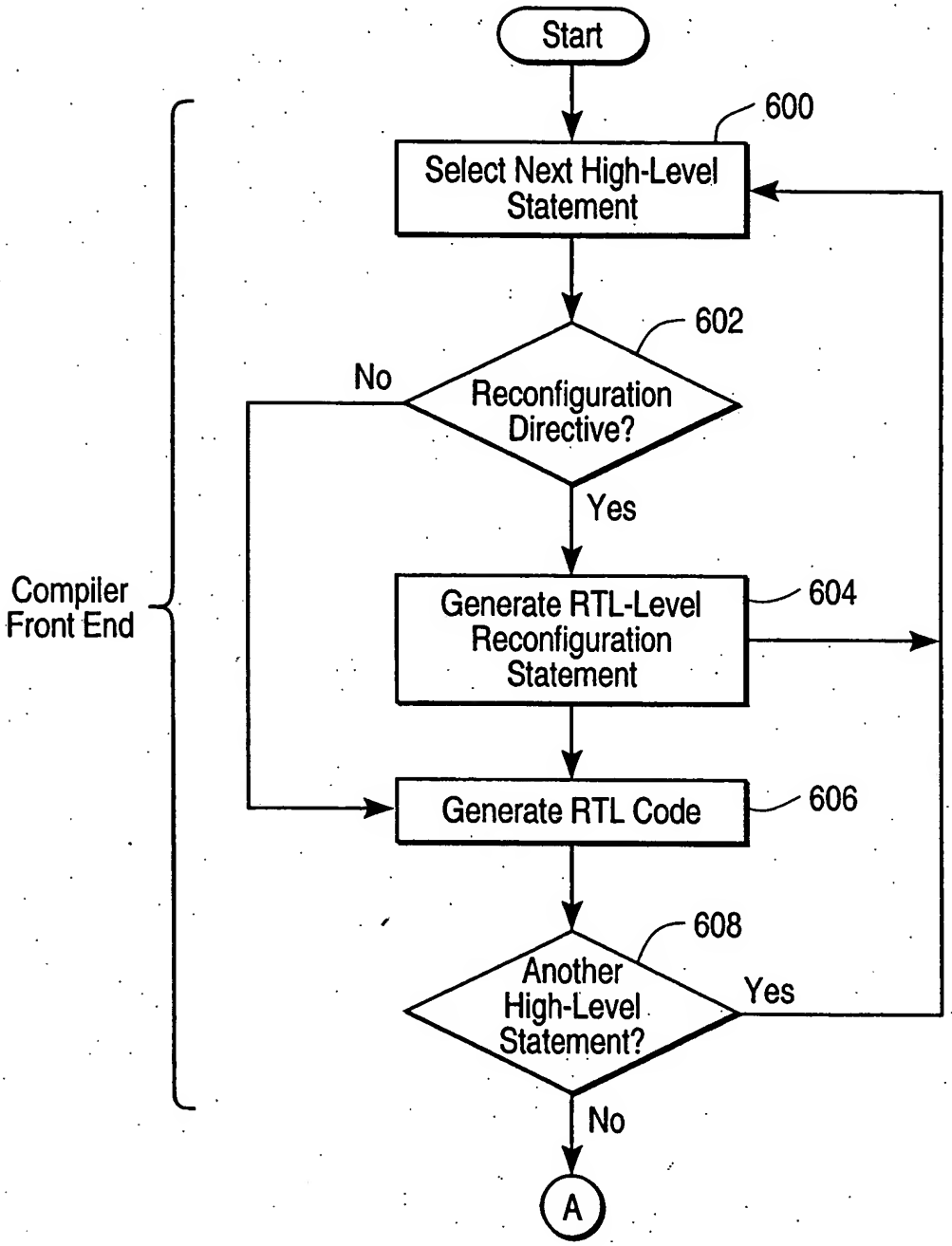
Start
600
Select Next High-Level Statement
602
No
Reconfiguration Directive?
Yes
Compiler Front End
Generate RTL-Level Reconfiguration Statement
604
Generate RTL Code
606
608
Another High-Level Statement?
Yes
No
A

FIG. 3C

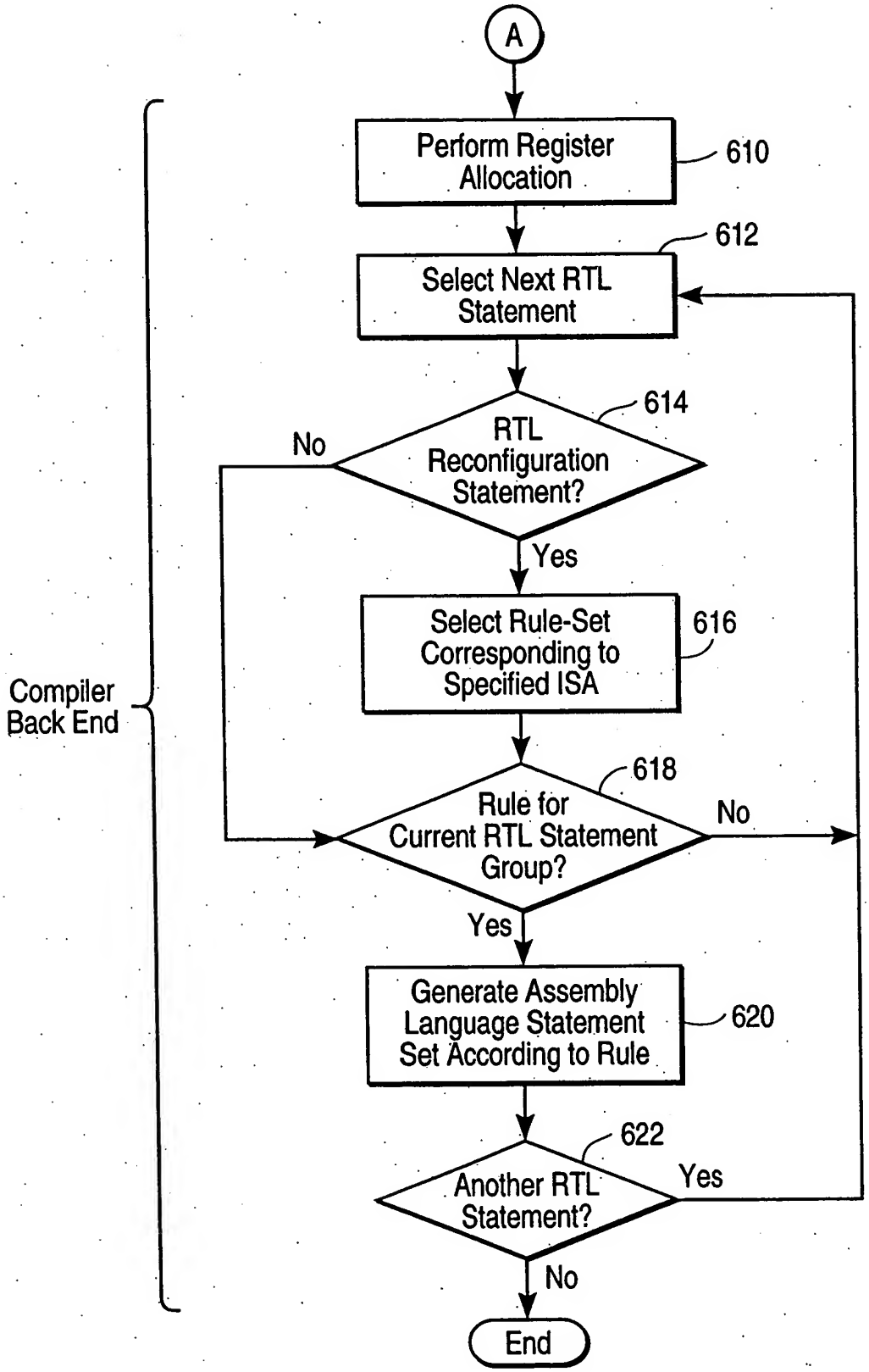
A
Perform Register Allocation
610
612
Select Next RTL Statement
614
RTL Reconfiguration Statement?
No
Yes
Select Rule-Set Corresponding to Specified ISA
616
618
Rule for Current RTL Statement Group?
No
Yes
Generate Assembly Language Statement Set According to Rule
620
622
Another RTL Statement?
Yes
No
End
Compiler Back End

FIG. 3D

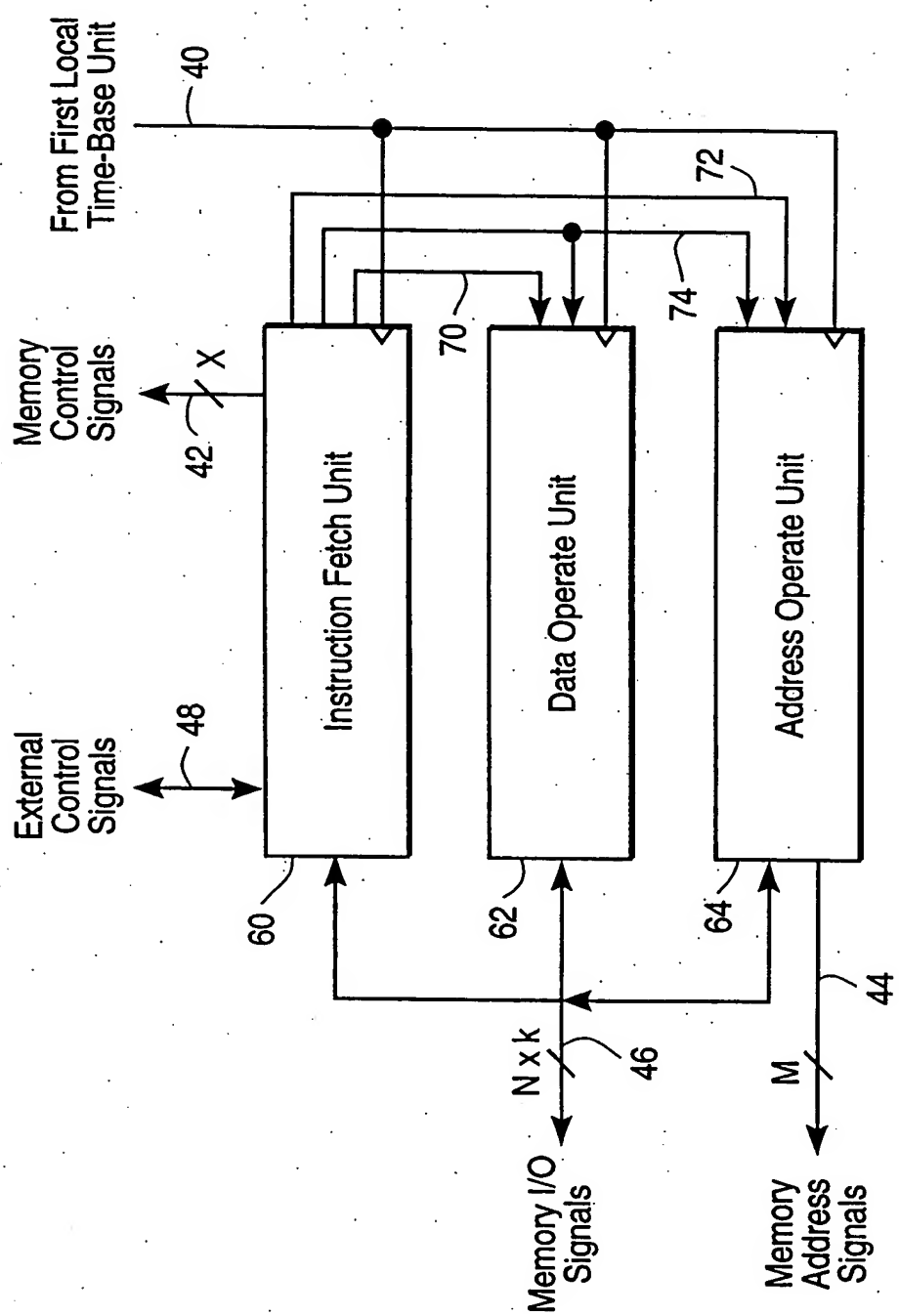
From First Local Time-Base Unit
40
72
74
70
Memory Control Signals
X
42
Instruction Fetch Unit
Data Operate Unit
Address Operate Unit
External Control Signals
48
60
62
64
44
N x k
46
M
Memory I/O Signals
Memory Address Signals
32

FIG. 4

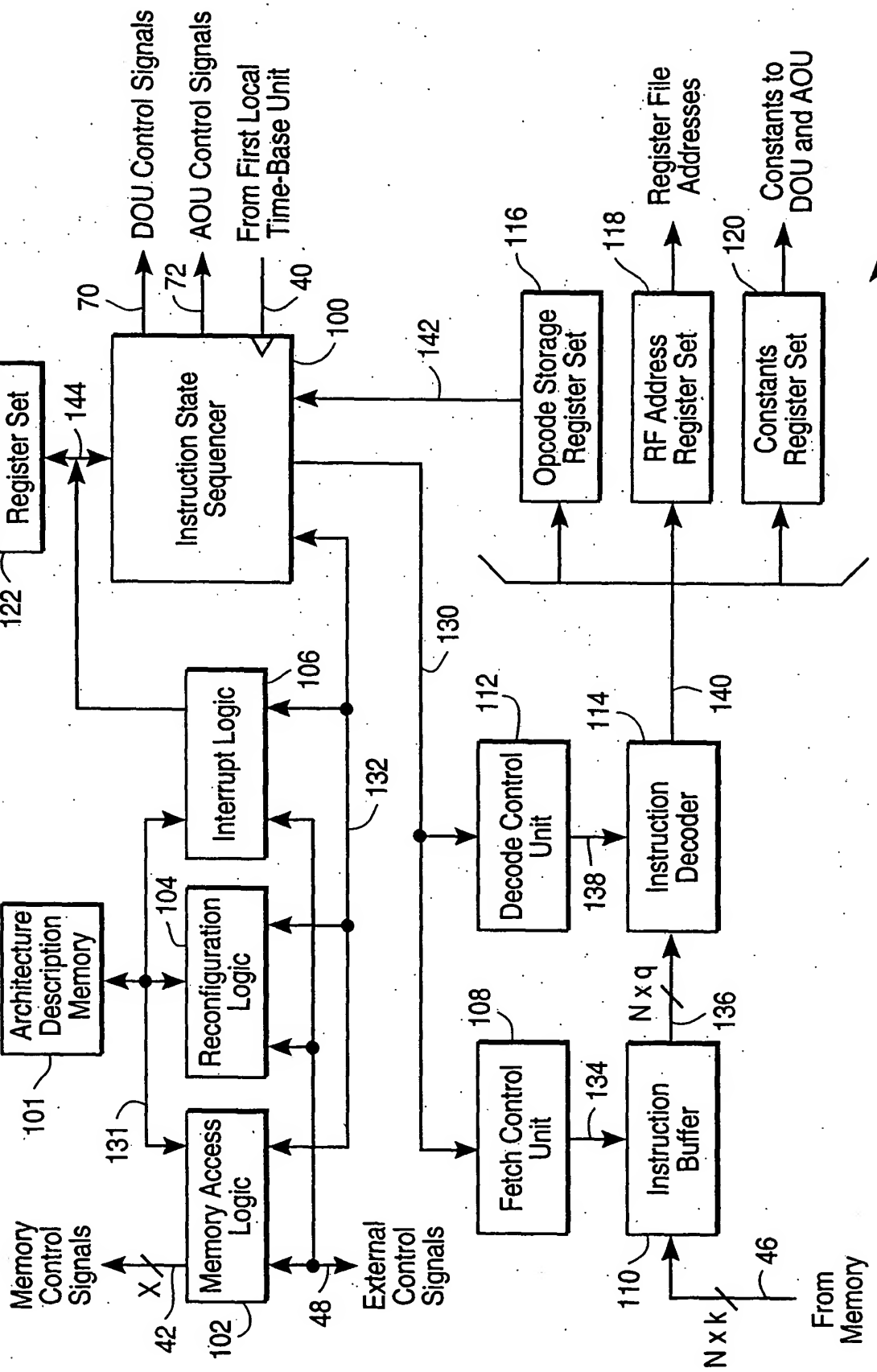
DOU Control Signals
AOU Control Signals
From First Local Time-Base Unit
Register File Addresses
Constants to DOU and AOU
70
72
40
60
Process Control Register Set
144
Instruction State Sequencer
100
142
Opcode Storage Register Set
116
RF Address Register Set
118
Constants Register Set
120
122
130
Interrupt Logic
106
132
Decode Control Unit
112
114
140
Instruction Decoder
Architecture Description Memory
101
104
Reconfiguration Logic
138
131
108
N x q
136
Memory Control Signals
X
Memory Access Logic
Fetch Control Unit
134
Instruction Buffer
42
102
48
External Control Signals
110
46
N x k
From Memory

FIG. 5

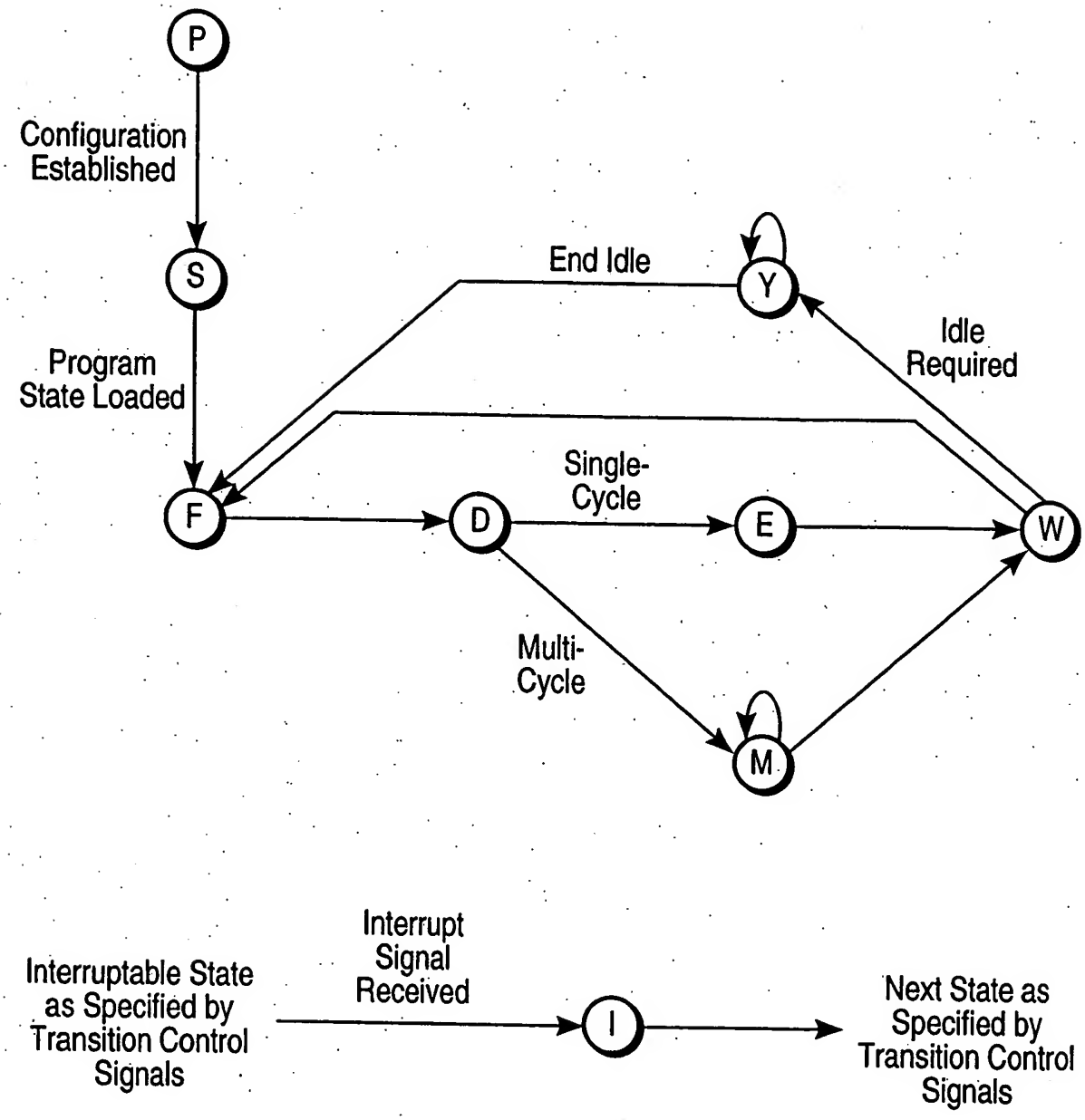
P
Configuration Established
S
Program State Loaded
End Idle
Y
Idle Required
F
D
Single-Cycle
E
W
Multi-Cycle
M
Interruptable State as Specified by Transition Control Signals
Interrupt Signal Received
I
Next State as Specified by Transition Control Signals

FIG. 6

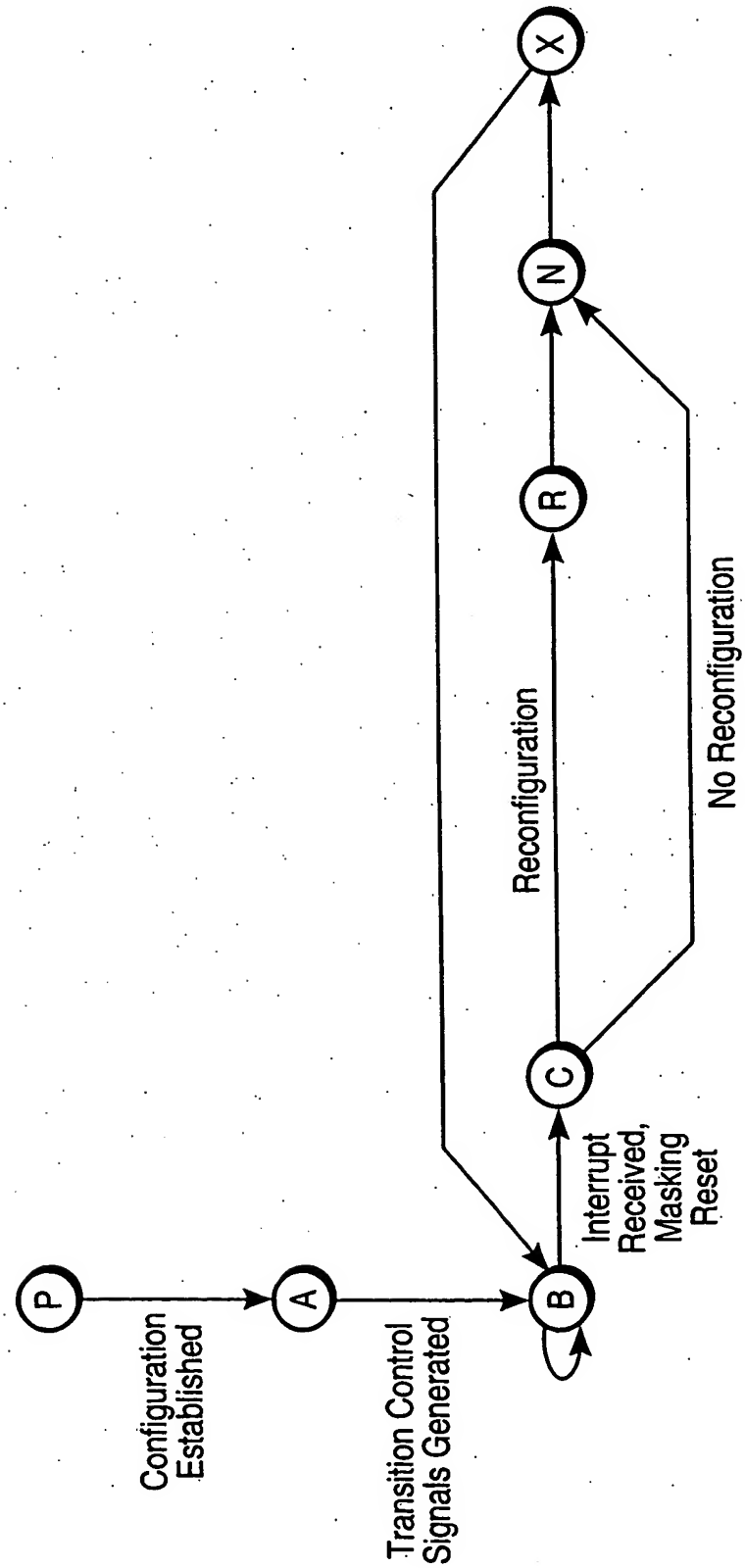
P
A
B
C
R
N
X
Configuration Established
Transition Control Signals Generated
Interrupt Received, Masking Reset
Reconfiguration
No Reconfiguration

FIG. 7

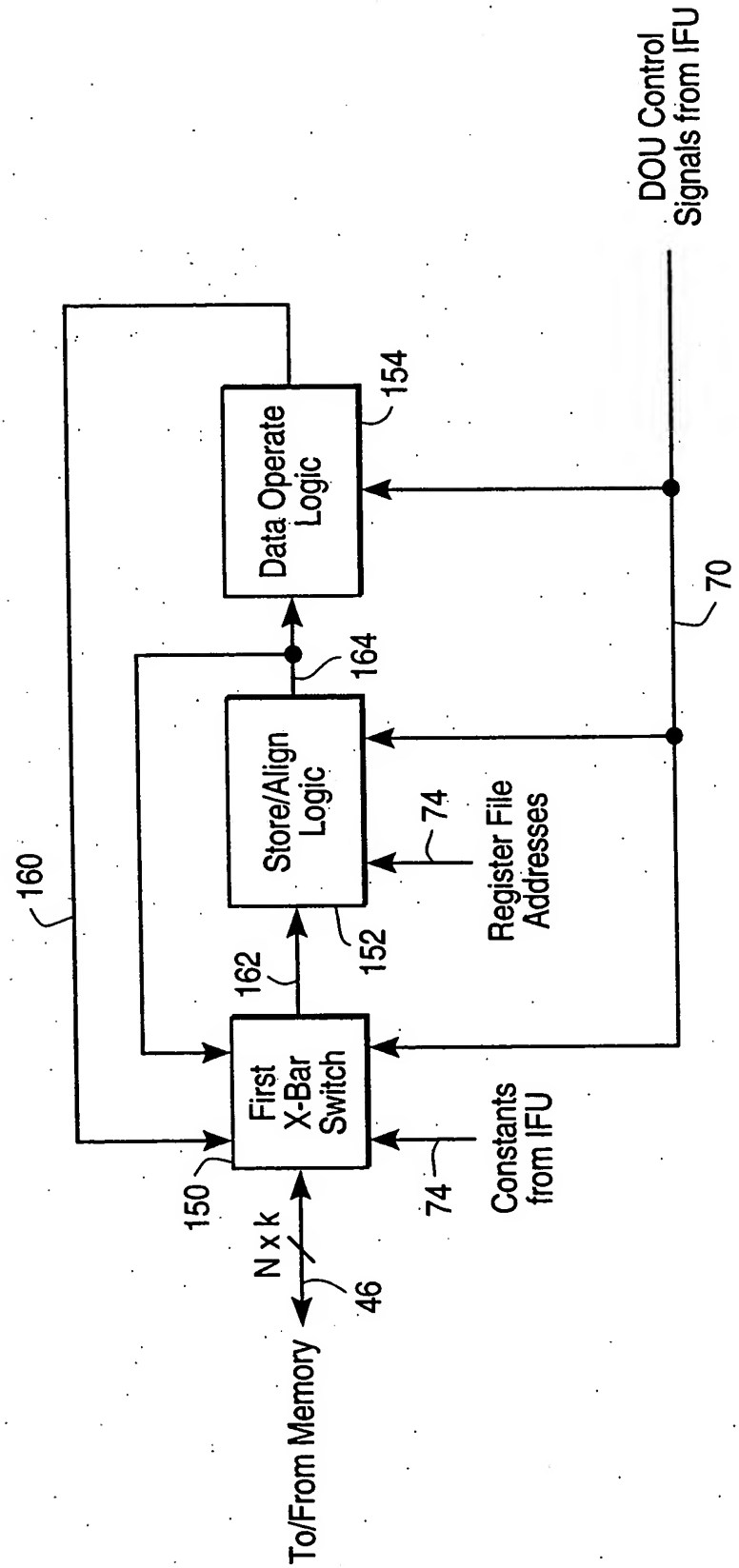
DOU Control Signals from IFU
Data Operate Logic
154
Store/Align Logic
164
Register File Addresses
74
First X-Bar Switch
Constants from IFU
74
N x k
46
To/From Memory
150
160
162
152
70
62

FIG. 8

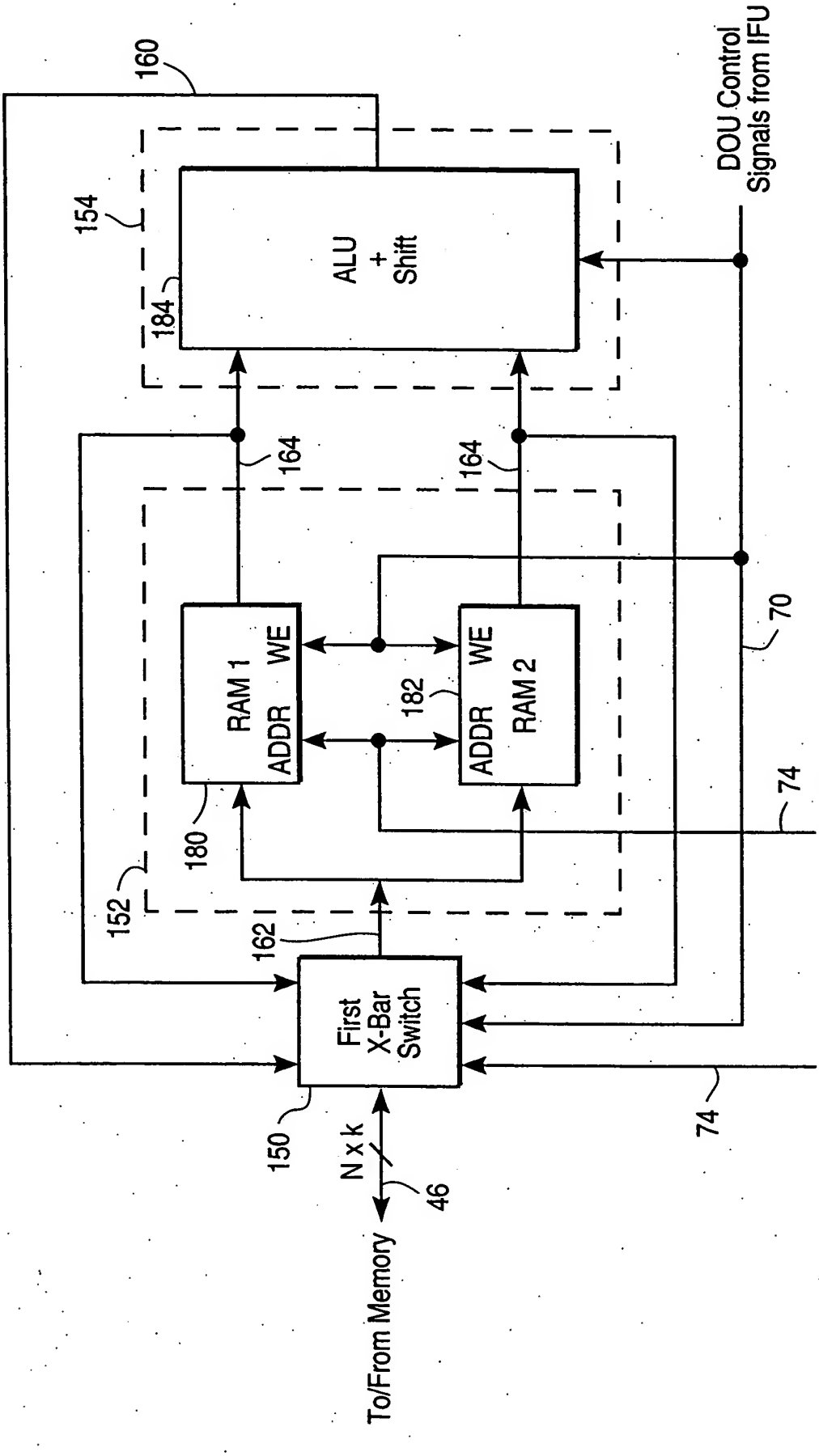
160
154
184
ALU
+
Shift
DOU Control
Signals from IFU
164
164
RAM 1
ADDR
WE
182
ADDR
WE
RAM 2
70
180
74
Register File
Addresses
152
162
First
X-Bar
Switch
Constants
from IFU
74
150
N x k
46
To/From Memory
61

FIG. 9A

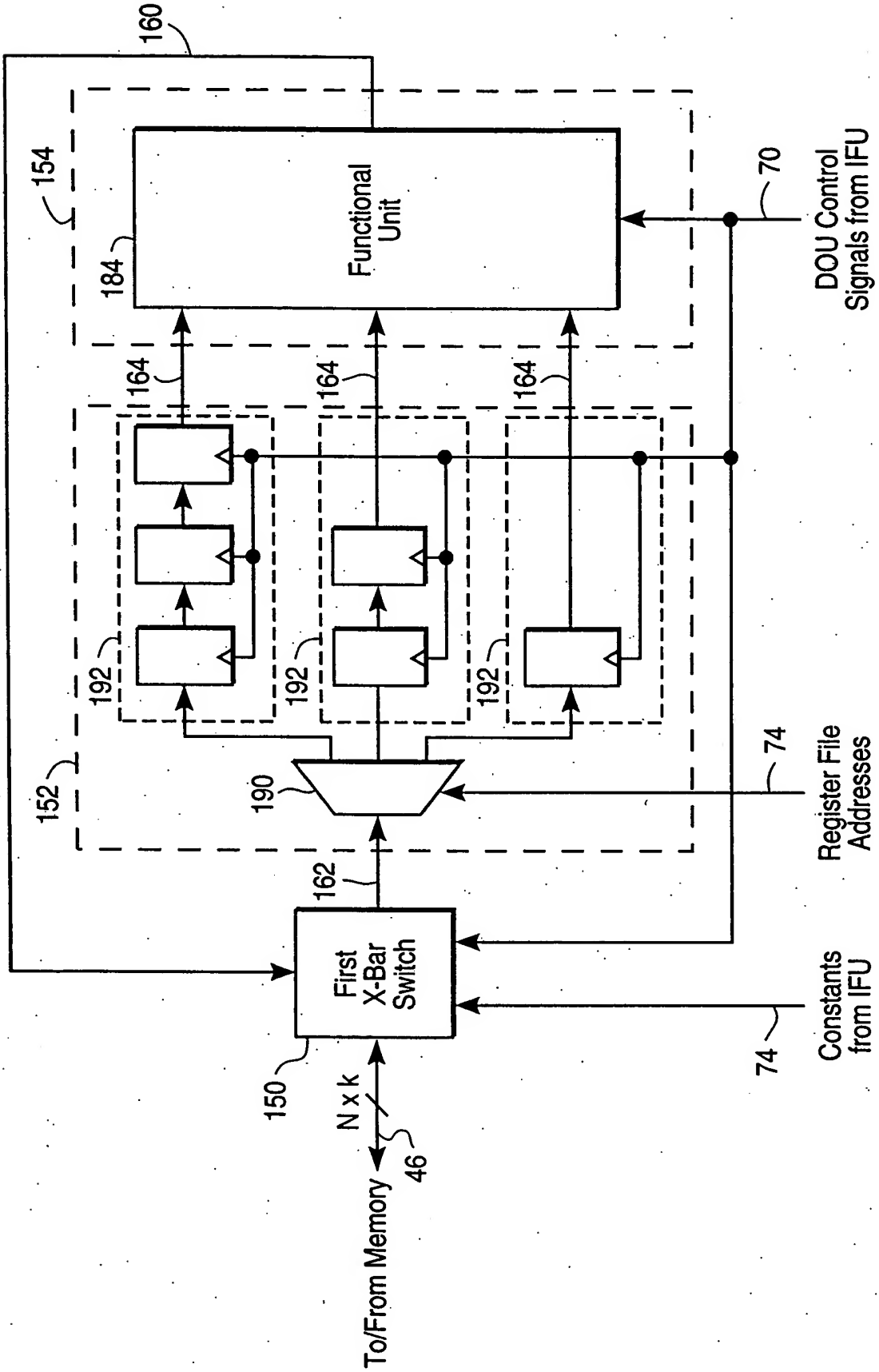
160
154
184
Functional Unit
70
DOU Control Signals from IFU
164
164
164
192
192
192
152
190
74
Register File Addresses
162
First X-Bar Switch
Constants from IFU
74
150
N x k
46
To/From Memory
63

FIG. 9B

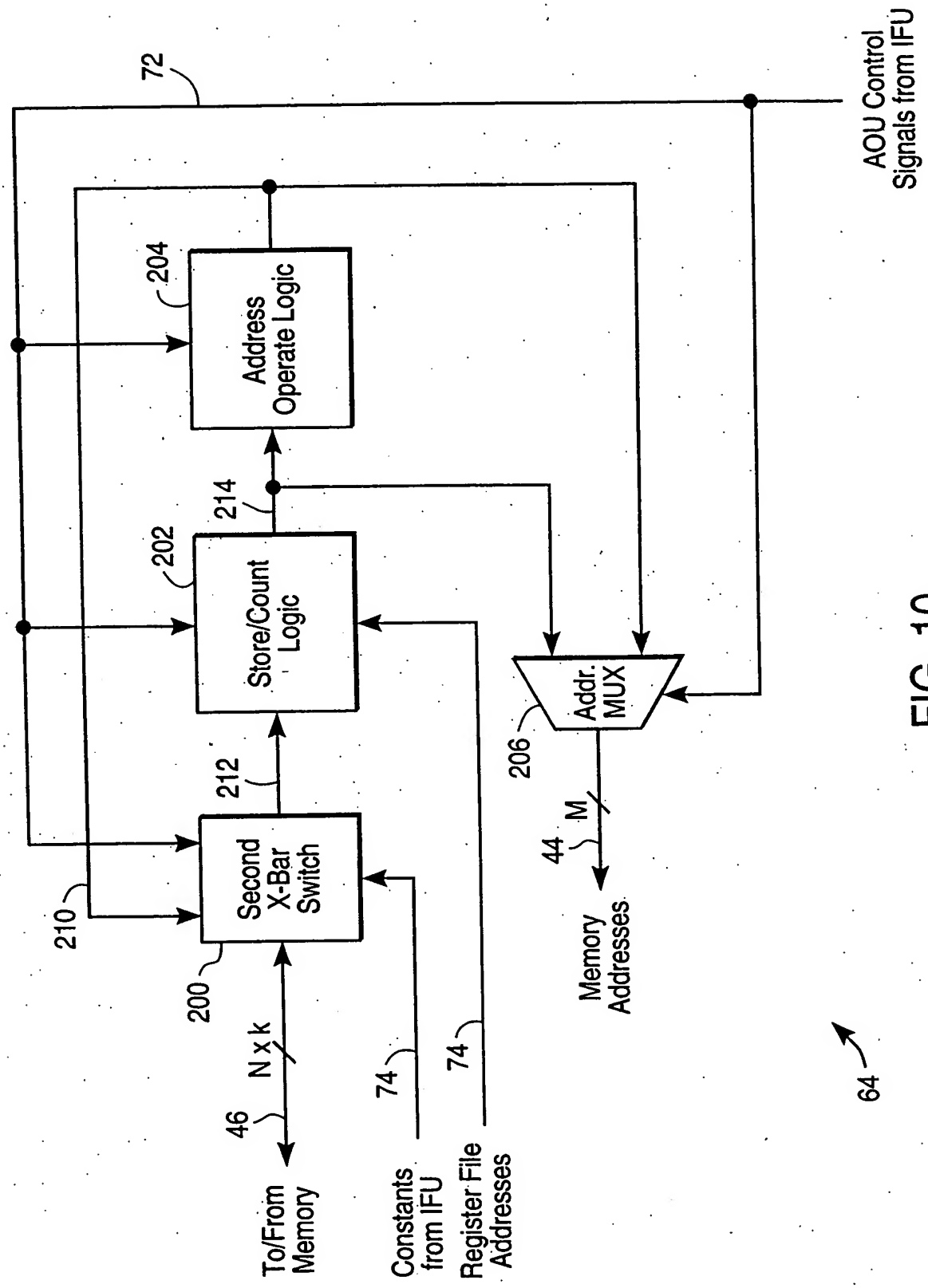
72
AOU Control Signals from IFU
204
Address Operate Logic
214
202
Store/Count Logic
212
Second X-Bar Switch
210
200
206
Addr. MUX
44
M
Memory Addresses
N x k
46
To/From Memory
74
Constants from IFU
74
Register File Addresses
64

FIG. 10

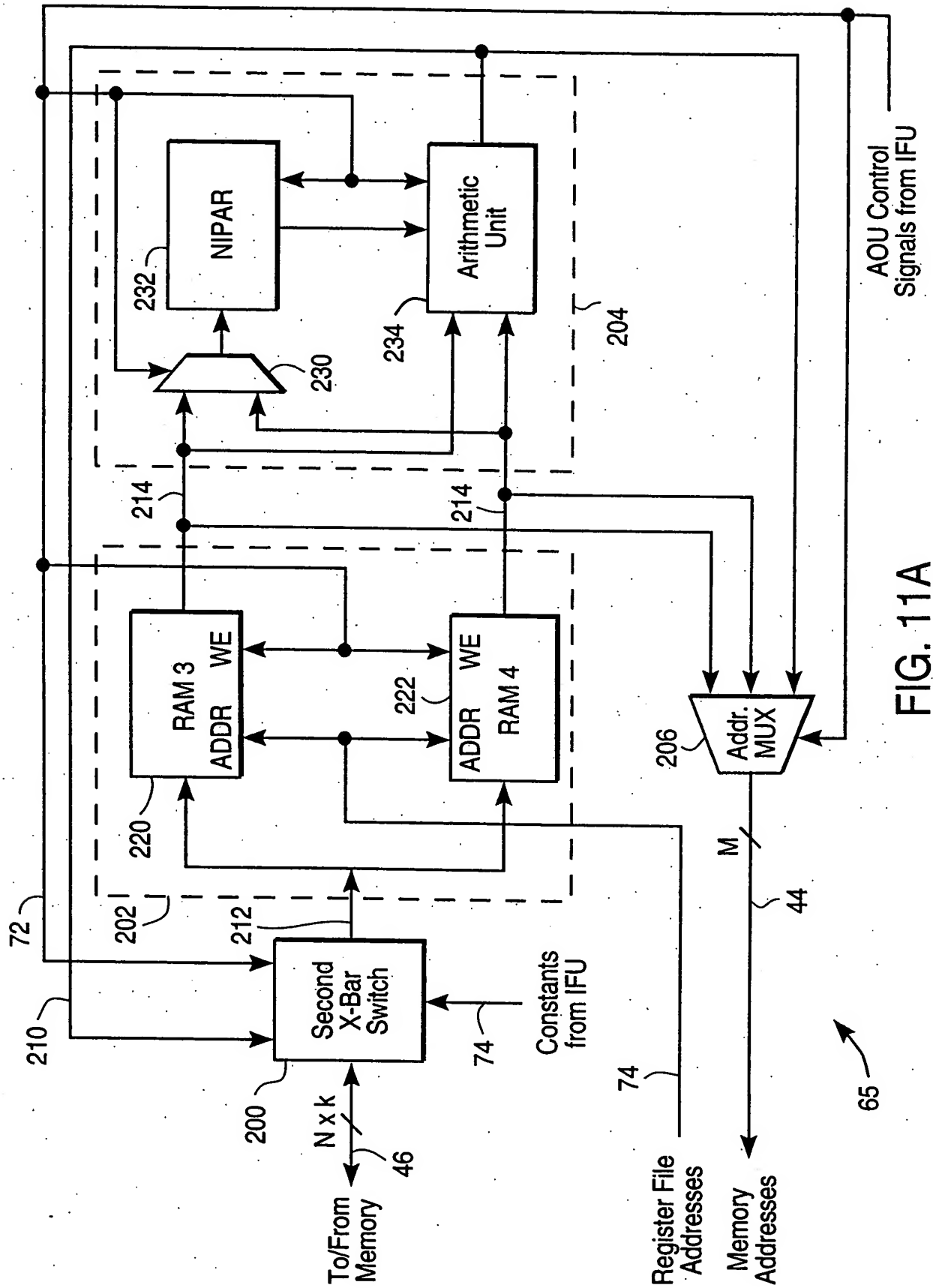
NIPAR
Arithmetic Unit
AOU Control Signals from IFU
232
234
230
204
214
214
RAM 3
ADDR WE
ADDR WE
RAM 4
222
220
206
Addr. MUX
M
44
72
202
212
210
Second X-Bar Switch
74
Constants from IFU
74
200
N x k
46
To/From Memory
Register File Addresses
Memory Addresses
65

FIG. 11A

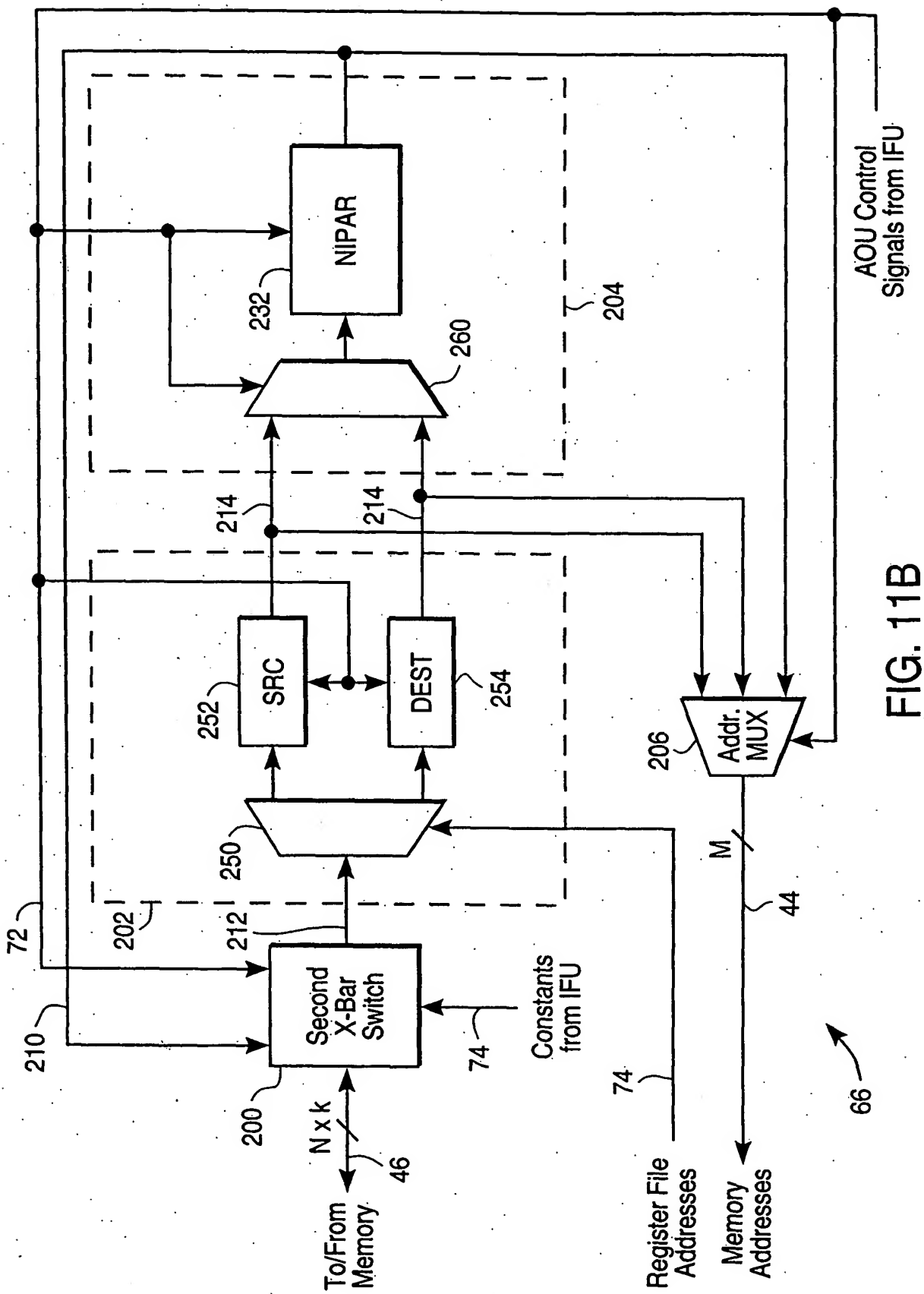
AOU Control Signals from IFU
NIPAR
232
204
260
214
214
SRC
DEST
252
254
206
Addr. MUX
250
M
44
72
202
212
Second X-Bar Switch
Constants from IFU
210
74
74
200
N x k
46
To/From Memory
Register File Addresses
Memory Addresses
66

FIG. 11B

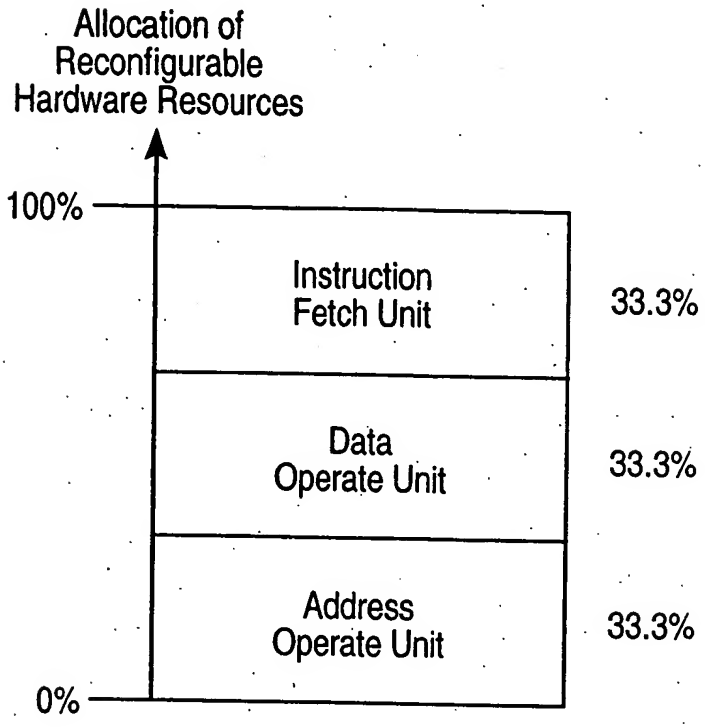

FIG. 12A

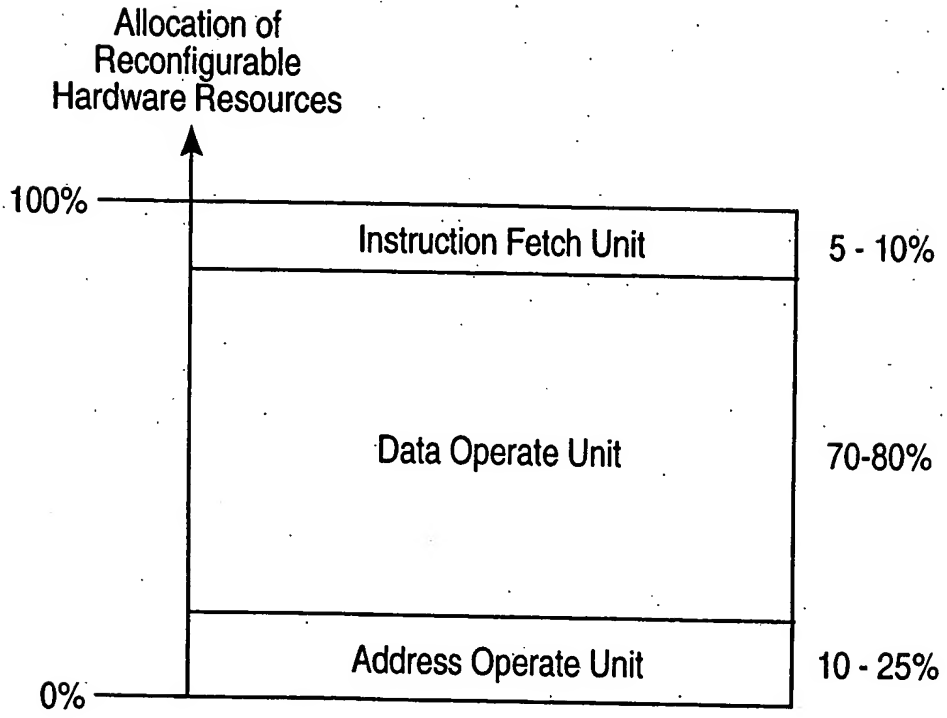

FIG. 12B

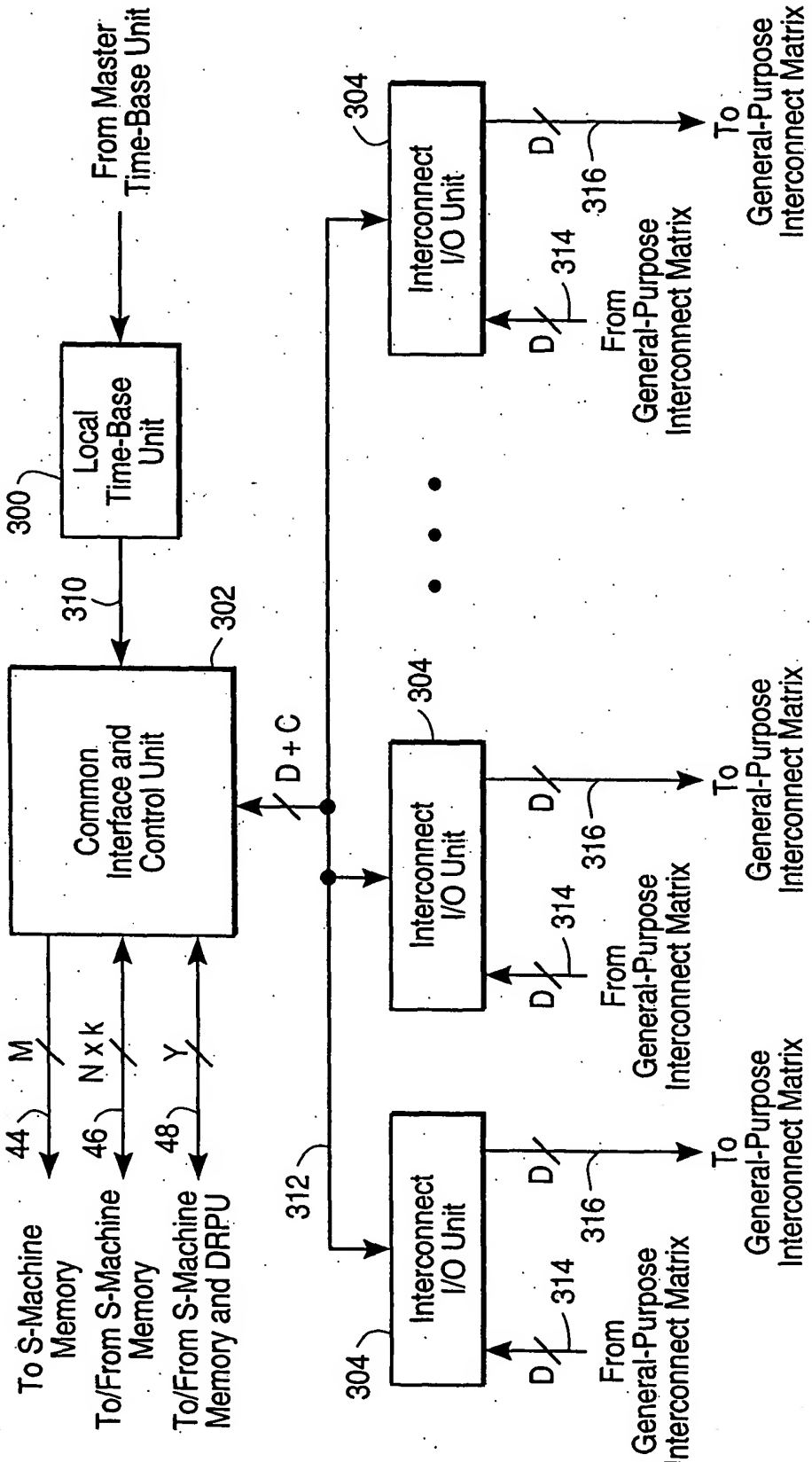
From Master Time-Base Unit
Local Time-Base Unit
300
310
Common Interface and Control Unit
302
D + C
312
304
Interconnect I/O Unit
D
314
316
From General-Purpose Interconnect Matrix
To General-Purpose Interconnect Matrix
M
N x k
Y
44
46
48
To S-Machine Memory
To/From S-Machine Memory
To/From S-Machine Memory and DRPU
14

FIG. 13

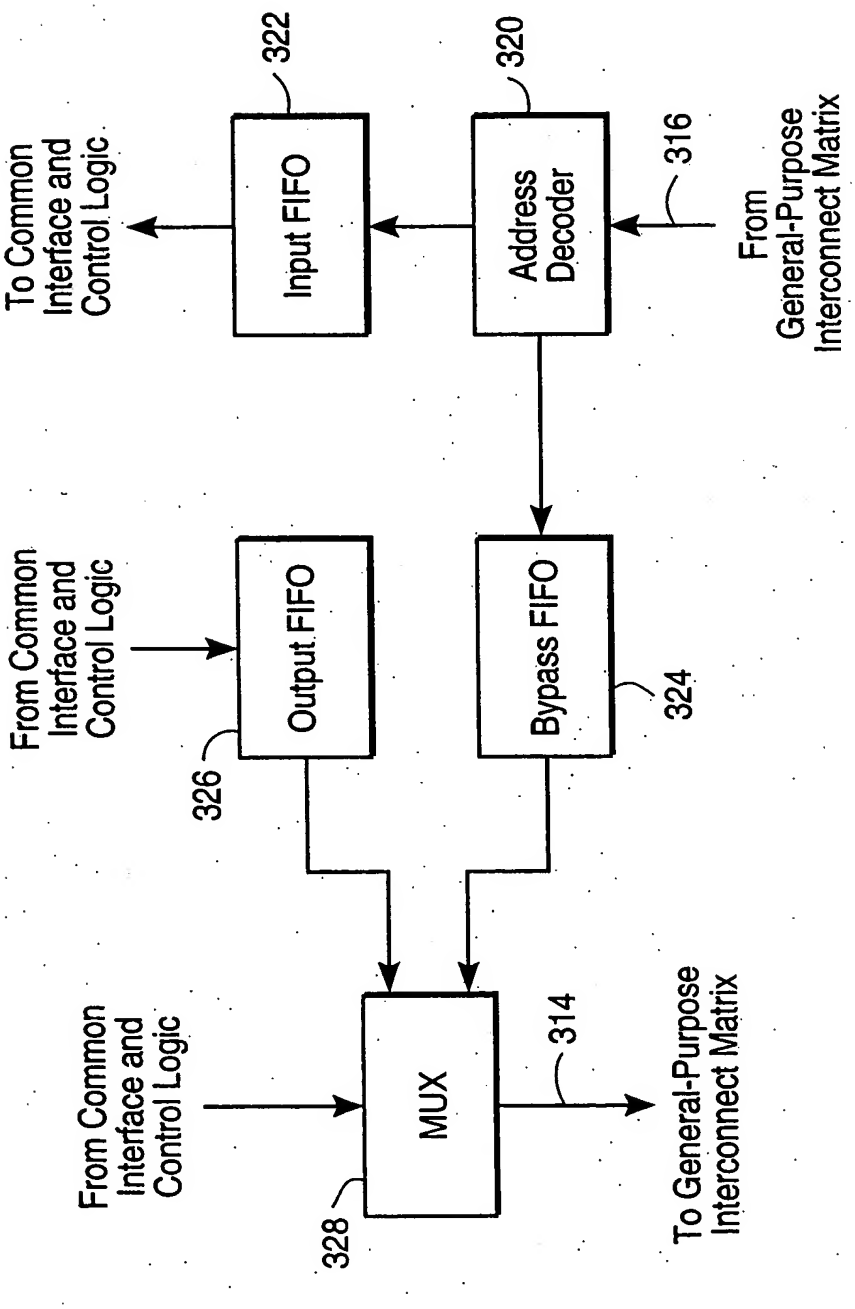
322
320
316
To Common Interface and Control Logic
Input FIFO
Address Decoder
From General-Purpose Interconnect Matrix
From Common Interface and Control Logic
Output FIFO
Bypass FIFO
324
326
From Common Interface and Control Logic
MUX
314
To General-Purpose Interconnect Matrix
328
304

FIG. 14

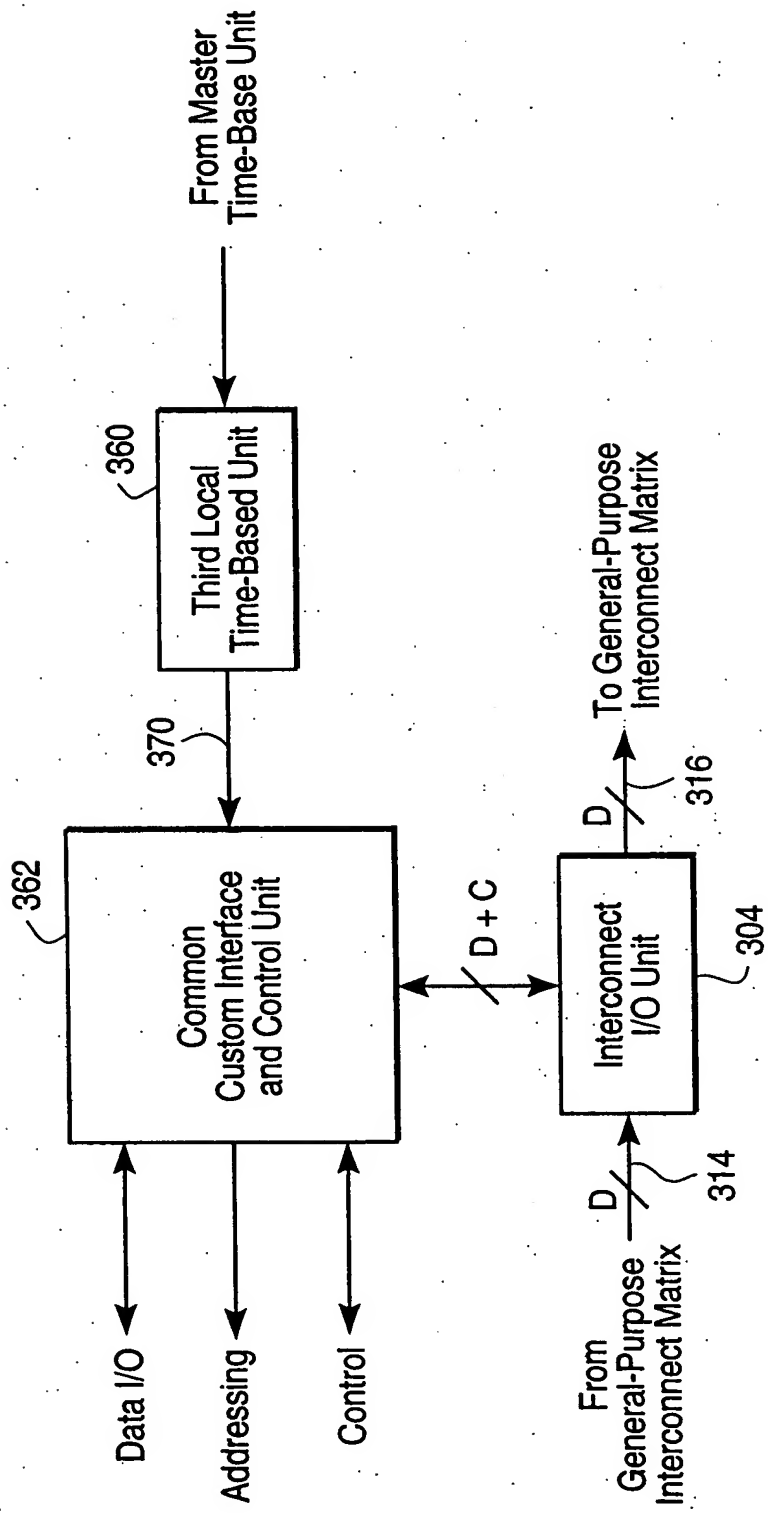
From Master Time-Base Unit
360
Third Local Time-Based Unit
370
362
Common Custom Interface and Control Unit
D + C
Interconnect I/O Unit
304
D
316
To General-Purpose Interconnect Matrix
D
314
From General-Purpose Interconnect Matrix
Data I/O
Addressing
Control
18

FIG. 15

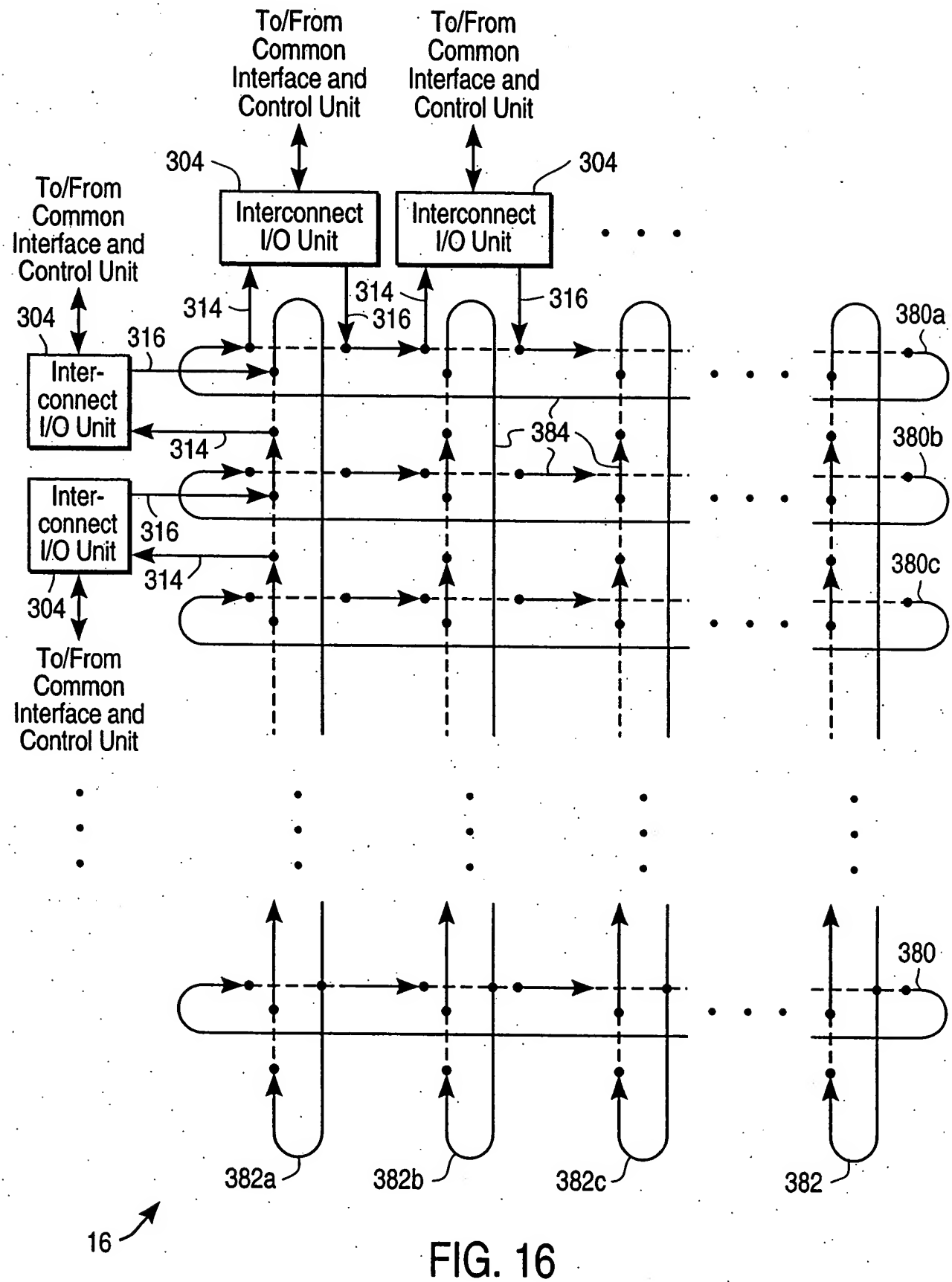
To/From Common Interface and Control Unit
To/From Common Interface and Control Unit
304
304
Interconnect I/O Unit
Interconnect I/O Unit
To/From Common Interface and Control Unit
304
316
314
314
316
316
380a
Inter-connect I/O Unit
314
384
380b
Inter-connect I/O Unit
316
314
380c
304
To/From Common Interface and Control Unit
380
382a
382b
382c
382
16

FIG. 16

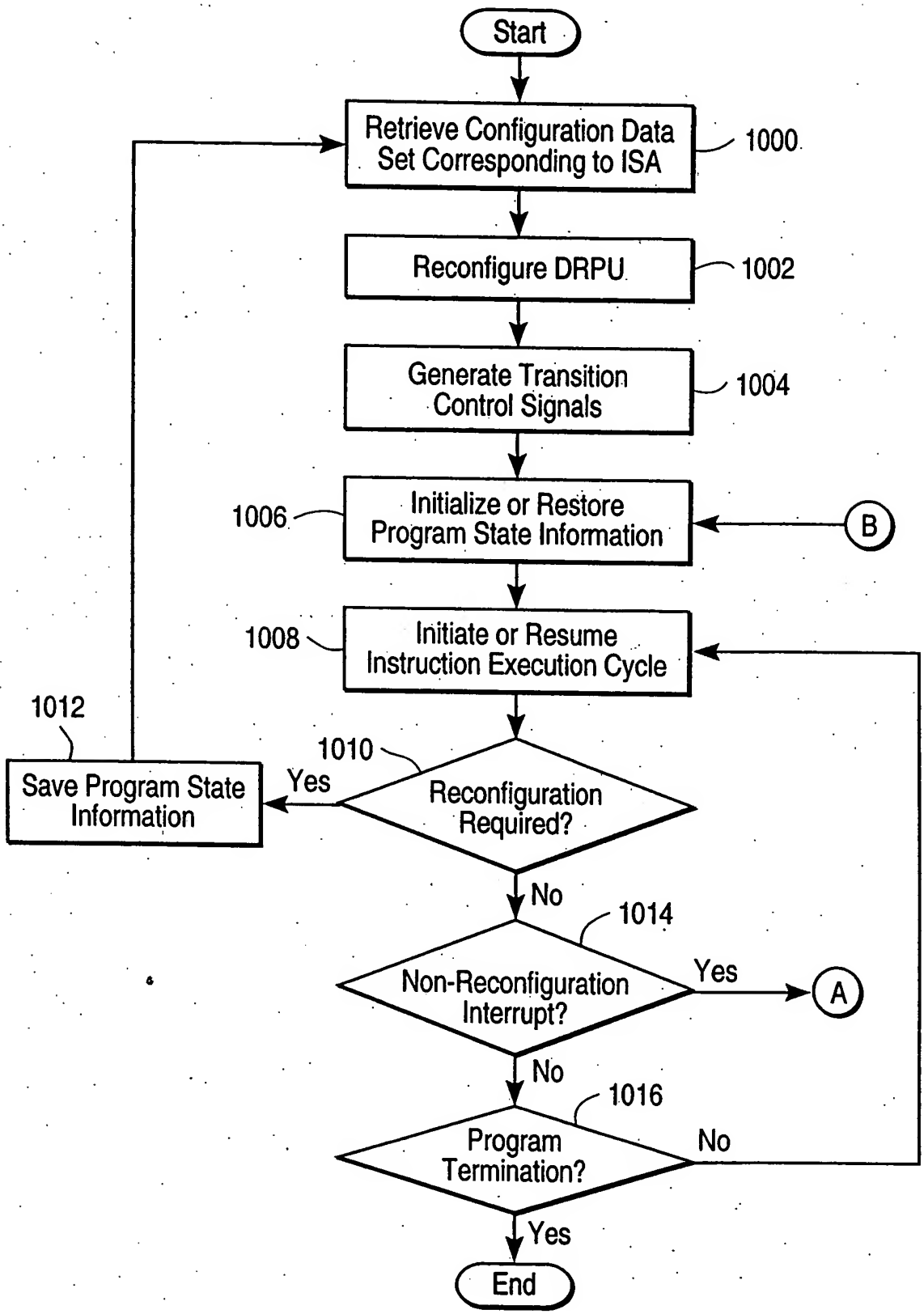
Start
Retrieve Configuration Data Set Corresponding to ISA
1000
Reconfigure DRPU
1002
Generate Transition Control Signals
1004
1006
Initialize or Restore Program State Information
B
1008
Initiate or Resume Instruction Execution Cycle
1012
1010
Save Program State Information
Yes
Reconfiguration Required?
No
1014
Non-Reconfiguration Interrupt?
Yes
A
No
1016
Program Termination?
No
Yes
End

FIG. 17A

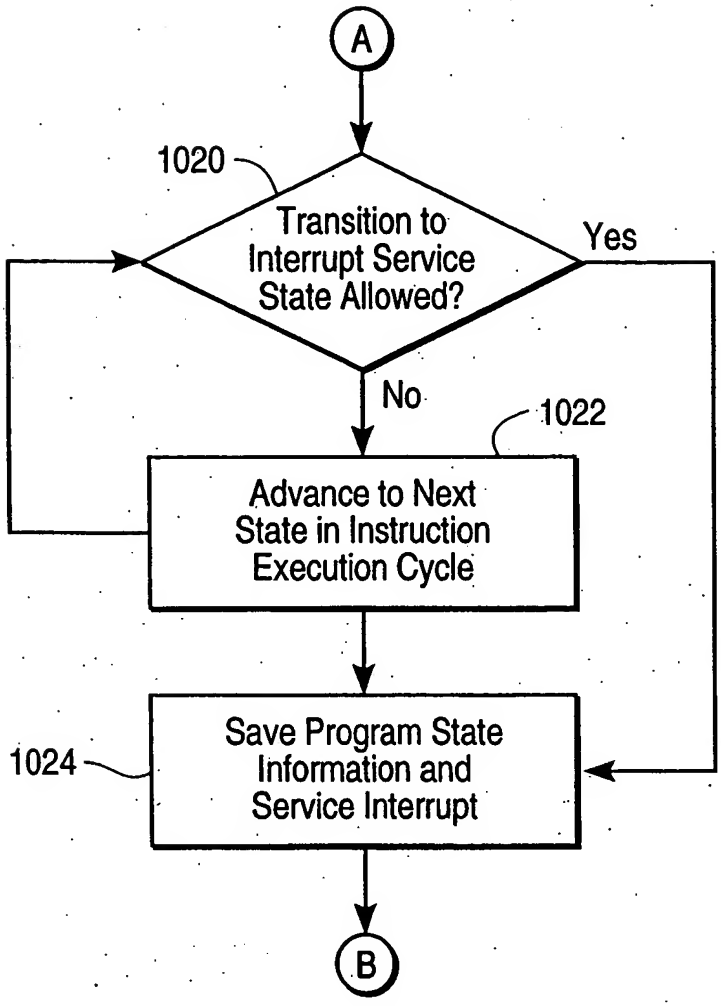
A
1020
Transition to Interrupt Service State Allowed?
Yes
No
1022
Advance to Next State in Instruction Execution Cycle
1024
Save Program State Information and Service Interrupt
B

FIG. 17B

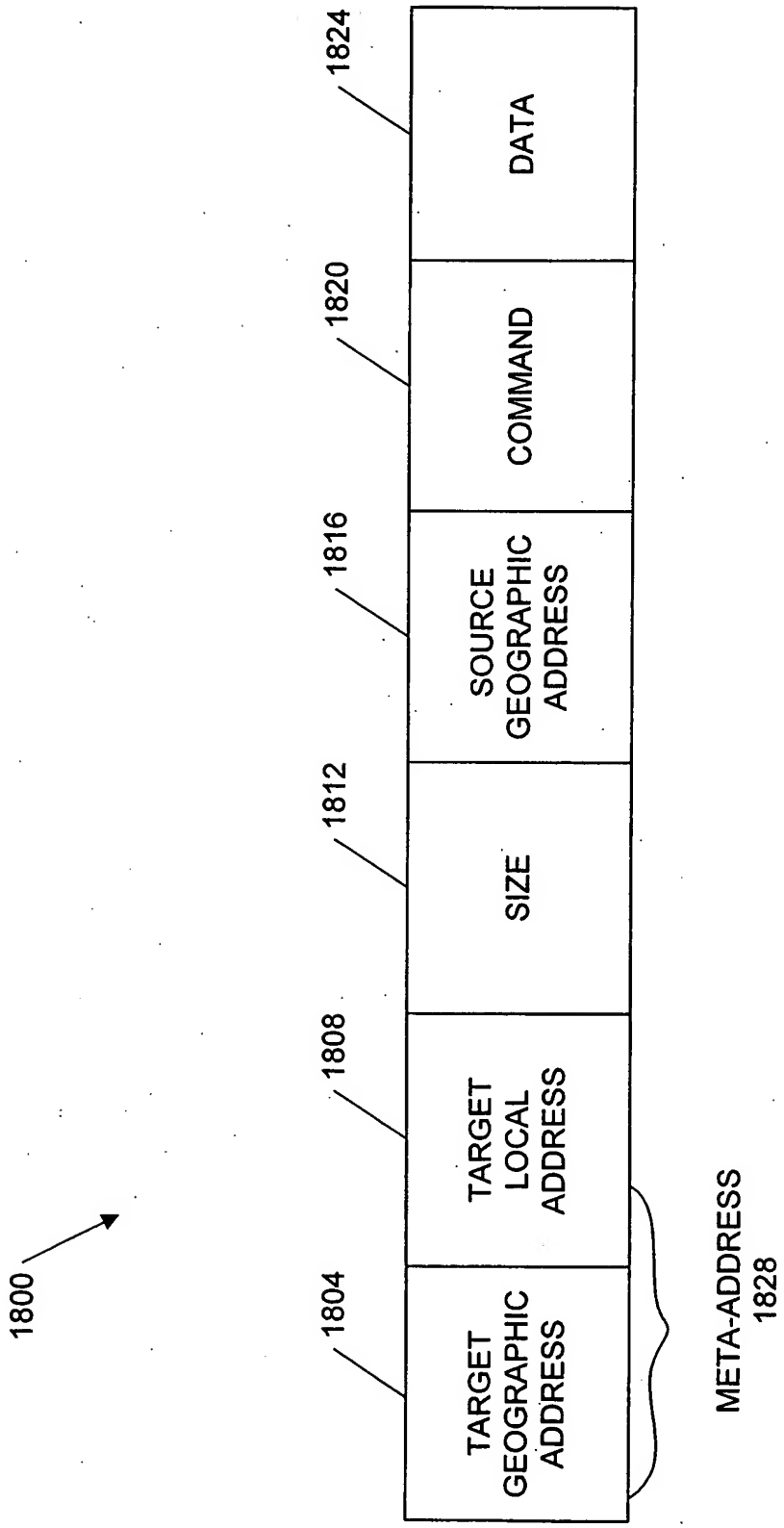
1800
1804
TARGET GEOGRAPHIC ADDRESS
1808
TARGET LOCAL ADDRESS
1812
SIZE
1816
SOURCE GEOGRAPHIC ADDRESS
1820
COMMAND
1824
DATA
META-ADDRESS
1828

FIGURE 18

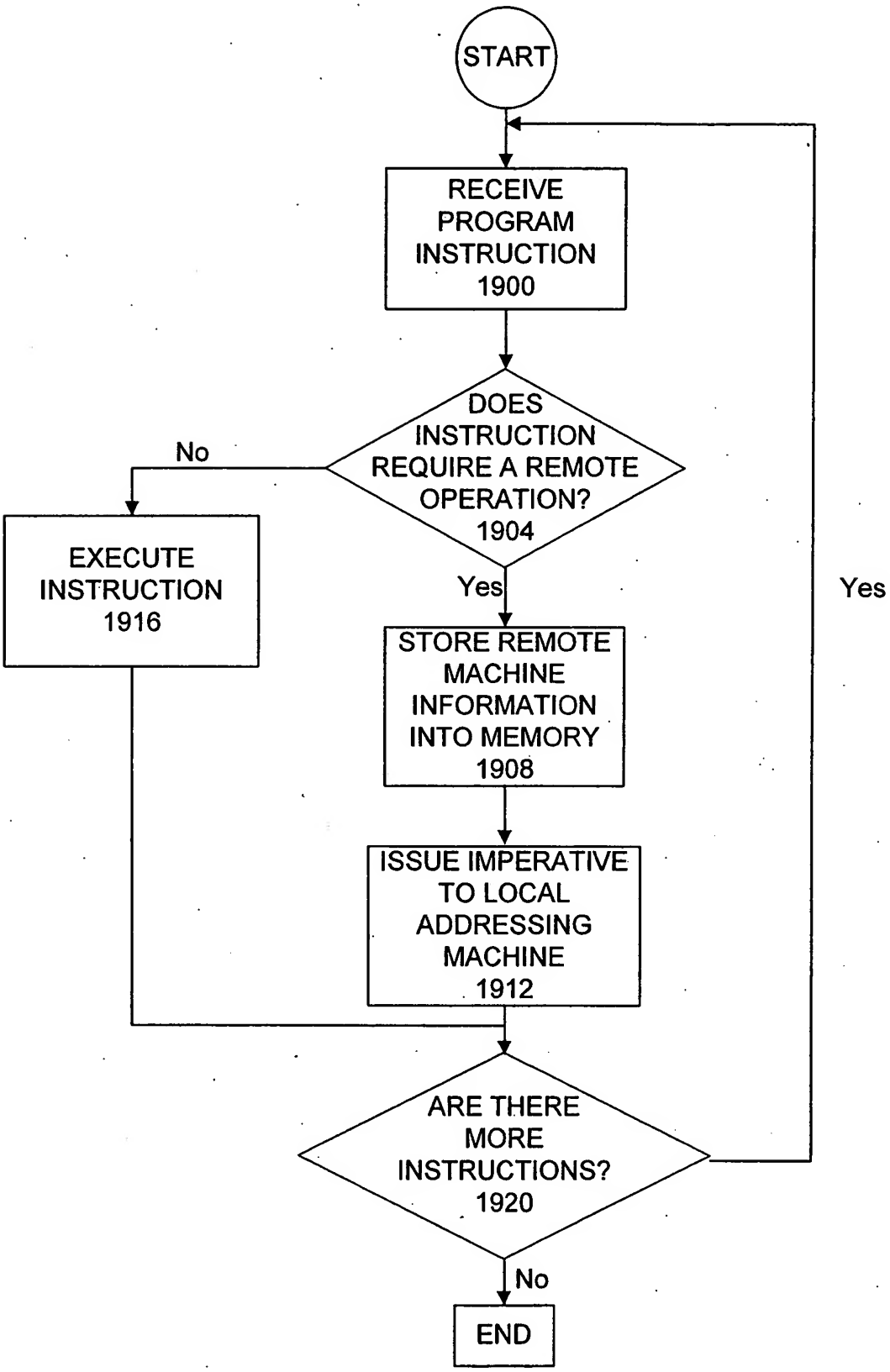
START
RECEIVE PROGRAM INSTRUCTION 1900
DOES INSTRUCTION REQUIRE A REMOTE OPERATION? 1904
No
Yes
EXECUTE INSTRUCTION 1916
STORE REMOTE MACHINE INFORMATION INTO MEMORY 1908
ISSUE IMPERATIVE TO LOCAL ADDRESSING MACHINE 1912
ARE THERE MORE INSTRUCTIONS? 1920
Yes
No
END

FIGURE 19

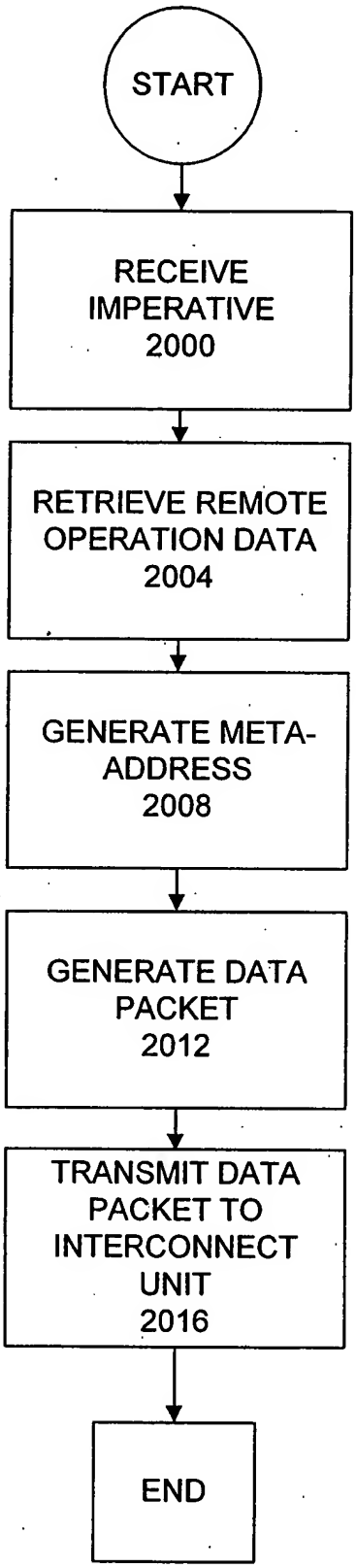
START
RECEIVE IMPERATIVE 2000
RETRIEVE REMOTE OPERATION DATA 2004
GENERATE META-ADDRESS 2008
GENERATE DATA PACKET 2012
TRANSMIT DATA PACKET TO INTERCONNECT UNIT 2016
END

FIGURE 20

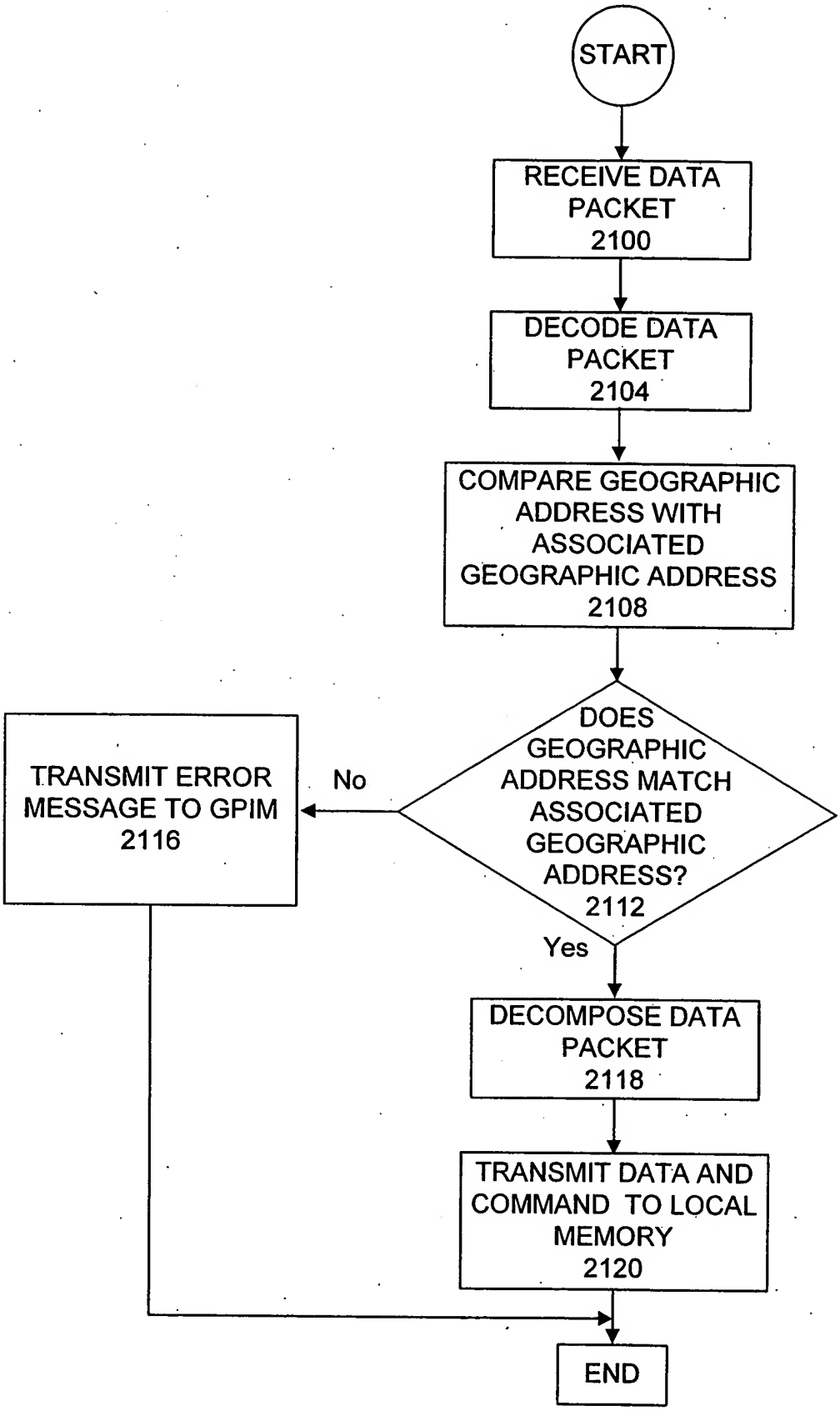
START
RECEIVE DATA PACKET 2100
DECODE DATA PACKET 2104
COMPARE GEOGRAPHIC ADDRESS WITH ASSOCIATED GEOGRAPHIC ADDRESS 2108
DOES GEOGRAPHIC ADDRESS MATCH ASSOCIATED GEOGRAPHIC ADDRESS? 2112
No
TRANSMIT ERROR MESSAGE TO GPIM 2116
Yes
DECOMPOSE DATA PACKET 2118
TRANSMIT DATA AND COMMAND TO LOCAL MEMORY 2120
END

FIGURE 21

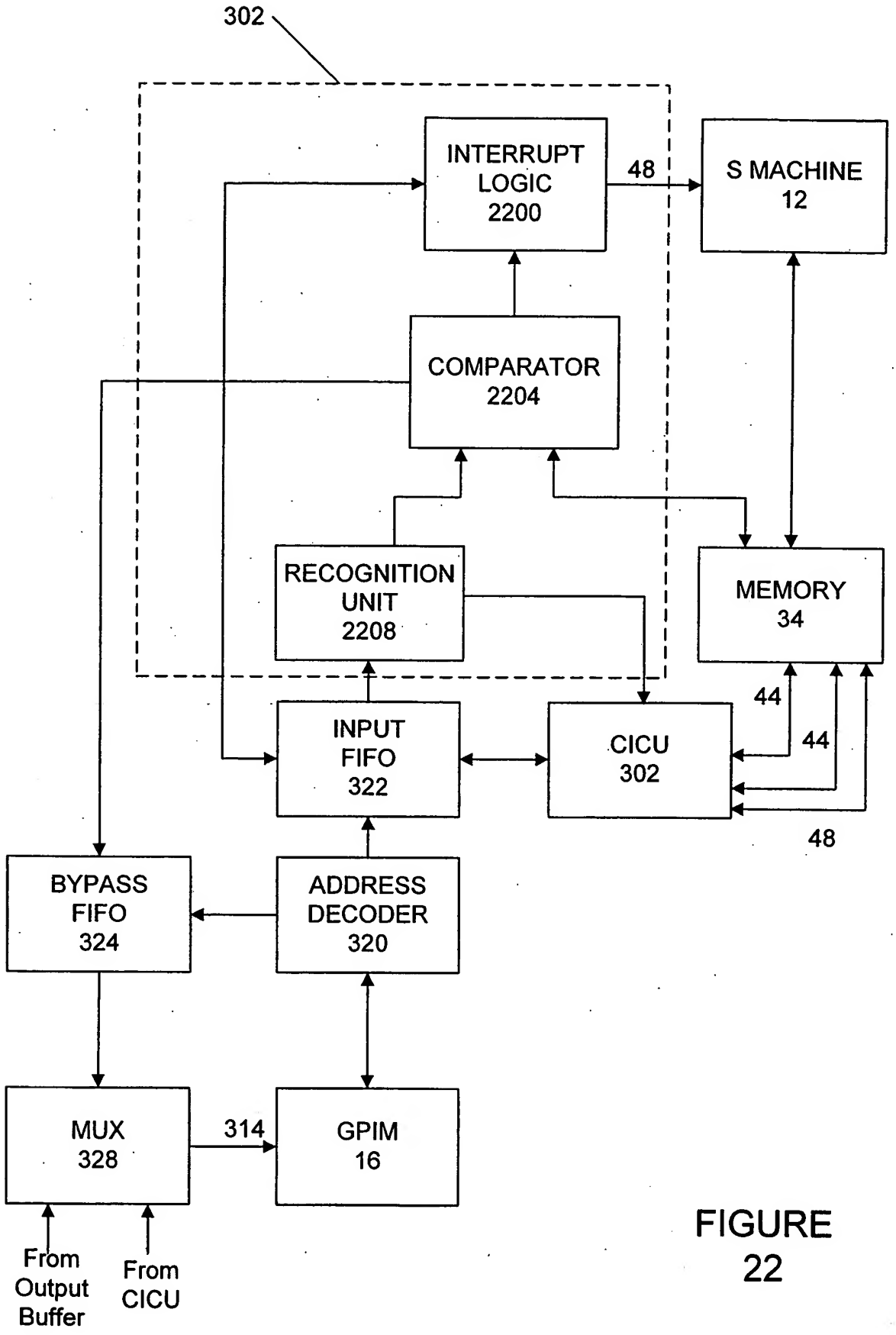
302
INTERRUPT LOGIC 2200
48
S MACHINE 12
COMPARATOR 2204
RECOGNITION UNIT 2208
MEMORY 34
44
44
INPUT FIFO 322
CICU 302
48
BYPASS FIFO 324
ADDRESS DECODER 320
MUX 328
314
GPIM 16
From Output Buffer
From CICU

FIGURE 22

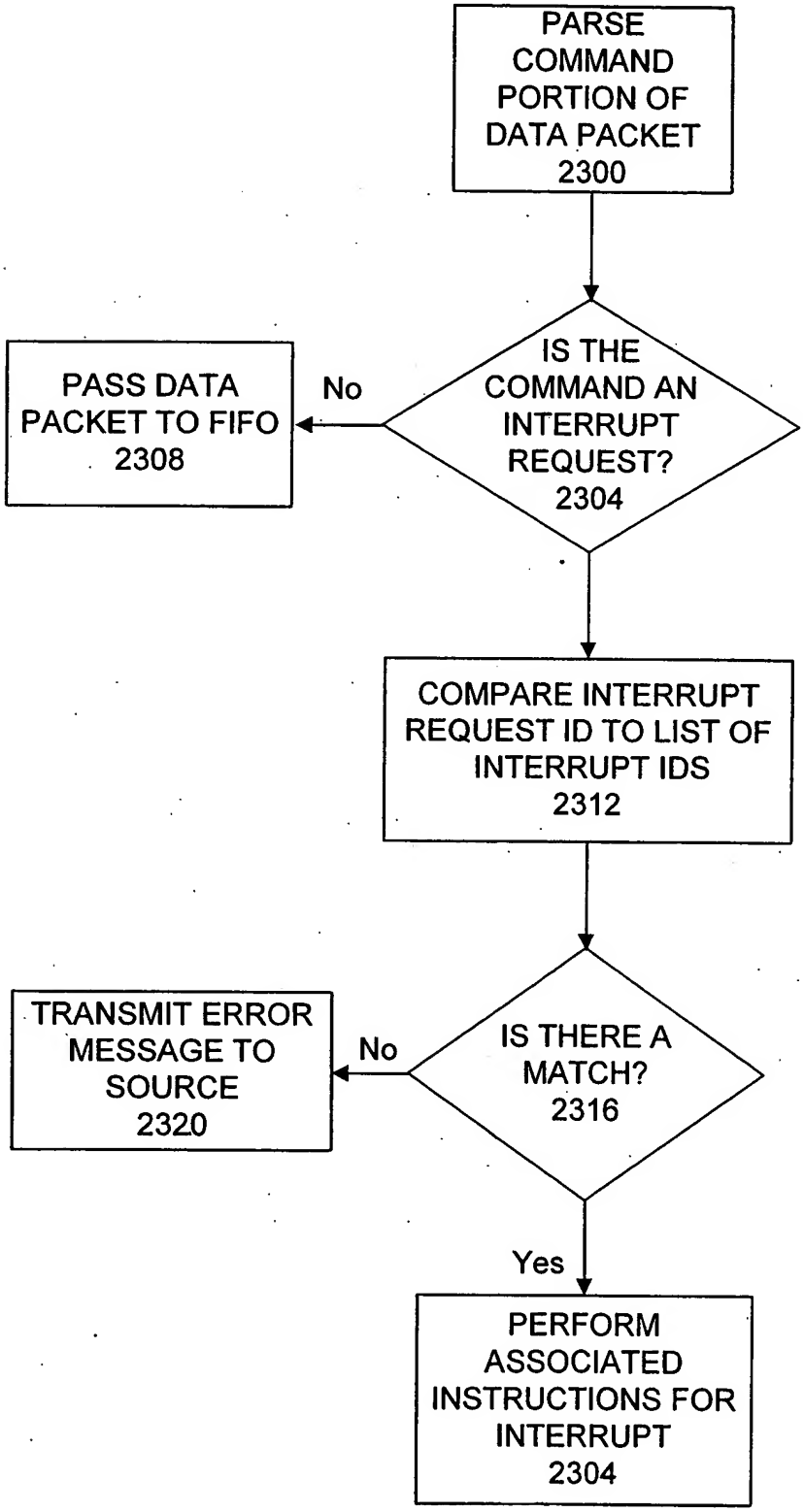
PARSE COMMAND PORTION OF DATA PACKET 2300
IS THE COMMAND AN INTERRUPT REQUEST? 2304
No
PASS DATA PACKET TO FIFO 2308
COMPARE INTERRUPT REQUEST ID TO LIST OF INTERRUPT IDS 2312
IS THERE A MATCH? 2316
No
TRANSMIT ERROR MESSAGE TO SOURCE 2320
Yes
PERFORM ASSOCIATED INSTRUCTIONS FOR INTERRUPT 2304

FIGURE 23